PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-079506
(43)Date of publication of application : 24.03.1998

(51)Int.Cl. H01L 29/78
H01L 21/336
H01L 21/265
H01L 21/8238
H01L 27/092

(21)Application number : 08-326507
(22)Date of filing : 06.12.1996

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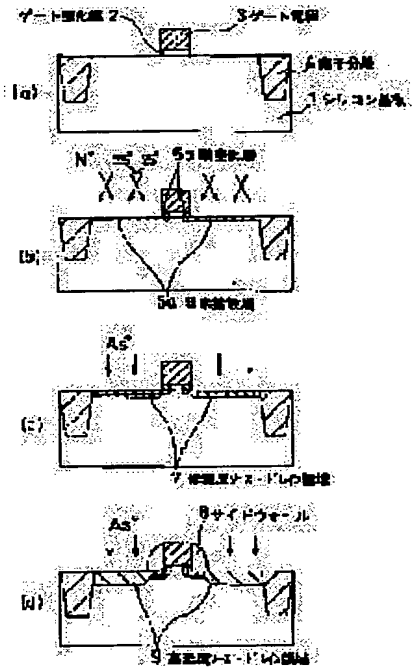
(30)Priority
Priority number : 08 20802 Priority date : 07.02.1996 Priority country : JP
08183004 12.07.1996 JP

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device, which is mounted with a MOS type field effect transistor of high performance and reliability, and its manufacturing method.
SOLUTION: A gate oxide film 2 and a gate electrode 3 are formed on a silicon substrate 1 in which an element separation 4 is formed. Then, nitrogen ions are implanted by large-inclination-ion-implantation method in four steps, in the direction inclined by 25° , and an acid nitride layer 5a is formed at both end parts of the gate oxide film 2, and a nitrogen-diffused layer 6a is formed in the silicon substrate 1. And then lightly doped source and drain areas 7 are formed by impurity ion implantation, and side walls 8 are formed on both side surfaces of the gate electrode 3, and then heavily doped source and drain regions 9 are formed by impurity ion implantation.



LEGAL STATUS

[Date of request for examination] 02.07.1999
[Date of sending the examiner's decision of rejection] 04.06.2002
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]

[Claim 1] In the semiconductor device which carried the MIS mold field-effect transistor on the semi-conductor substrate the above-mentioned MIS mold field-effect transistor The active region formed in some above-mentioned semi-conductor substrates, and the gate oxide formed on the above-mentioned active region, The gate electrode formed on the above-mentioned gate oxide, and the source field and drain field which introduced the impurity into the field located in both above-mentioned gate electrodes among the above-mentioned active regions, and was formed in it, The semiconductor device characterized by having the acid nitrated case formed in the edge by the side of the above-mentioned drain field at least among the both ends of the above-mentioned gate oxide.

[Claim 2] It is the semiconductor device characterized by forming the above-mentioned acid nitrated case in the both ends of the above-mentioned gate oxide in a semiconductor device according to claim 1.

[Claim 3] The semiconductor device characterized by having further the nitrogen diffusion layer formed in a part of drain field at least among the above-mentioned source field and the drain field in a semiconductor device according to claim 1.

[Claim 4] It is the semiconductor device characterized by forming the above-mentioned nitrogen diffusion layer in a semiconductor device according to claim 3 more shallowly than the above-mentioned source field and a drain field.

[Claim 5] In the semiconductor device according to claim 1, it has the nMIS mold field-effect transistor and the pMIS mold field-effect transistor on the semi-conductor substrate. The above-mentioned MIS mold field-effect transistor It is the above-mentioned nMIS mold field-effect transistor. The above-mentioned pMIS mold field-effect transistor The active region formed in some above-mentioned semi-conductor substrates, and the gate oxide formed on the above-mentioned active region, It has the gate electrode formed on the above-mentioned gate oxide, and the source field and drain field which

introduced the impurity into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and was formed in it. It is the semiconductor device characterized by not forming the acid nitrated case at the gate oxide of the above-mentioned pMIS mold field-effect transistor.

[Claim 6] It is the semiconductor device characterized by having further the nitrogen diffusion layer by which the above-mentioned nMIS mold field-effect transistor and the pMIS mold field-effect transistor were formed at least in the part in the above-mentioned source field and a drain field in the semiconductor device according to claim 5.

[Claim 7] It is the semiconductor device characterized by forming the above-mentioned nitrogen diffusion layer in a semiconductor device according to claim 6 more shallowly than any of the above-mentioned source field and a drain field.

[Claim 8] The semiconductor device characterized by having further the gate top insulator layer by which patterning was carried out to the above-mentioned gate electrode and coincidence on the above-mentioned gate electrode in a semiconductor device according to claim 1, 2, 3, 4, 5, 6, or 7.

[Claim 9] The semiconductor device characterized by having the nitrogen diffusion layer containing the nitrogen introduced into the semi-conductor substrate, the impurity diffused layer which is formed in the above-mentioned semi-conductor substrate, and contains the 1st conductivity-type impurity for carrier generation, and the field containing a part of above-mentioned impurity diffused layer [at least] in the condition that the defect resulting from the collision with a semi-conductor atom does not exceed detection level.

[Claim 10] While it sets to a semiconductor device according to claim 9 and the concentration of the above-mentioned 1st conductivity-type impurity in the above-mentioned impurity diffused layer decreases toward the method of the back of the above-mentioned semi-conductor substrate from the maximum concentration location of the field near the front face in a semi-conductor substrate The semiconductor device by which it is having-the distribution to which reduction rate becomes small in field which is large until the reduction rate arrives at predetermined location of the lower part which passed through above-mentioned maximum concentration location, and goes to method of the back rather than above-mentioned predetermined location characterized.

[Claim 11] The maximum concentration location of the 1st conductivity-type impurity in a semiconductor device

according to claim 9 or 10, have further the silicide film formed on the above-mentioned impurity diffused layer, and above-mentioned [in the above-mentioned impurity diffused layer] is a semiconductor device characterized by being in the method of directly under of an interface with the above-mentioned silicide film.

[Claim 12] In a semiconductor device according to claim 9 or 10 the above-mentioned semiconductor device The gate dielectric film formed on the active region in a semi-conductor substrate, and the gate electrode formed on this gate dielectric film, The source field and drain field which are formed in the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and contain the 1st conductivity-type impurity, It is the MIS mold field-effect transistor which has the channel field which is formed between the above-mentioned source field and a drain field among the above-mentioned active regions, and contains the 2nd conductivity-type impurity. The above-mentioned nitrogen diffusion layer the semiconductor device characterized by being formed in a field including the above-mentioned source field and a part of each drain field [at least].

[Claim 13] The sidewall which consists of an insulating ingredient formed on the both-sides side of the above-mentioned gate electrode in a semiconductor device according to claim 12, It has further the extension field which is formed, respectively between the above-mentioned source field and a drain field, and the direct lower part field of the above-mentioned gate electrode, and contains the low-concentration 1st conductivity-type impurity rather than the above-mentioned source field and a drain field. The above-mentioned nitrogen diffusion layer is a semiconductor device characterized by being continued and formed also in the above-mentioned extension field.

[Claim 14] It is the semiconductor device characterized by the above-mentioned nitrogen diffusion layer covering the above-mentioned channel field in a semiconductor device according to claim 12 or 13.

[Claim 15] the semiconductor device with which concentration of the above-mentioned impurity for carrier generation be characterize by the thing which enter into the above-mentioned channel field side to the case that there be no above-mentioned nitrogen , in the field near the front face in the above-mentioned semi-conductor substrate , and which , on the other hand , consist of methods of the back so that it keep away from a channel field side among the above-mentioned source field and a drain field in a semiconductor device according to claim 12 in the part

which adjoin the above-mentioned channel field by the field more than [a predetermined value] .

[Claim 16] the conductor which be formed on the above-mentioned source field and the above-mentioned drain field in the semiconductor device according to claim 12, 13, 14, or 15 and which contain a metal at least -- the maximum concentration location of the above-mentioned impurity for carrier generation in the field in which be further equipped with a film and the above-mentioned nitrogen diffusion layer be formed among the above-mentioned source field and the drain field -- the above -- a conductor -- the semiconductor device characterize by to be near an interface with a film .

[Claim 17] In a semiconductor device according to claim 9 the above-mentioned semiconductor device The emitter region which is formed in a part of active region in the above-mentioned semi-conductor substrate, and contains the 2nd conductivity-type impurity, The base region which is formed so that the above-mentioned emitter region may be surrounded in the above-mentioned active region, and contains the 1st conductivity-type impurity, It is the semiconductor device characterized by being formed in the field to which it is the bipolar transistor which has the collector field which is formed in the field which contains the lower part of the above-mentioned base region in the above-mentioned active region, and contains the 2nd conductivity-type impurity, and the above-mentioned nitrogen diffusion layer includes a part of above-mentioned emitter region [at least].

[Claim 18] In a semiconductor device according to claim 9 the above-mentioned semiconductor device The emitter region which is formed in a part of active region in the above-mentioned semi-conductor substrate, and contains the 2nd conductivity-type impurity, The base region which is formed so that the above-mentioned emitter region may be surrounded in the above-mentioned active region, and contains the 1st conductivity-type impurity, It is the semiconductor device characterized by being formed in the field to which it is the bipolar transistor which has the collector field which is formed in the field which contains the lower part of the above-mentioned base region in the above-mentioned active region, and contains the 2nd conductivity-type impurity, and the above-mentioned nitrogen diffusion layer includes a part of above-mentioned base region [at least].

[Claim 19] In the manufacture approach of a semiconductor device of having carried the MIS mold field-effect transistor the 1st process which forms the isolation surrounding an active region on a semi-conductor substrate, and

the above-mentioned active-region top -- an oxide film and a conductor -- with the 2nd process which deposits the film the above-mentioned oxide film and a conductor -- patterning of the film being carried out and with the 3rd process which forms the gate oxide and the gate electrode of the above-mentioned MIS mold field-effect transistor, respectively The 4th process which introduces nitrogen into the edge by the side of a drain field at least among the both ends of the above-mentioned gate oxide, and forms an acid nitrated case, The manufacture approach of the semiconductor device characterized by having the 5th process which introduces the 1st conductivity-type impurity into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and forms the source field and drain field of the above-mentioned MIS mold field-effect transistor in it.

[Claim 20] It is the manufacture approach of the semiconductor device characterized by forming the above-mentioned acid nitrated case by pouring in nitrogen ion from the direction which performs the 4th process of the above before the 5th process of the backward above of the 3rd process of the above, and includes the direction of the substrate upper part which inclined to the drain field side at least in the manufacture approach of a semiconductor device according to claim 19.

[Claim 21] The manufacture approach of the semiconductor device characterized by pouring in impurity ion from at least two or more directions which include the direction which inclined to the above-mentioned drain side at the 4th process of the above, and the direction leaning to the above-mentioned source field side in the manufacture approach of a semiconductor device according to claim 19.

[Claim 22] In the manufacture approach of a semiconductor device according to claim 20 or 21 The manufacture approach of the semiconductor device characterized by pouring in impurity ion from the direction to which 10 degrees or more inclined at the 4th process of the above to the direction vertical to the front face of the above-mentioned semi-conductor substrate in the cross section parallel to the direction of a channel of the above-mentioned transistor.

[Claim 23] It is the manufacture approach of the semiconductor device characterized by being carried out by heat-treating the above-mentioned semi-conductor substrate in the gas ambient atmosphere in which the 4th process of the above contains nitrogen at least in the manufacture approach of a semiconductor device according to claim 19.

[Claim 24] It is the manufacture

approach of the semiconductor device characterized by performing the 4th process of the above in an ammonia gas ambient atmosphere in the manufacture approach of a semiconductor device according to claim 23.

[Claim 25] It is the manufacture approach of the semiconductor device characterized by being carried out by generating the plasma in the gas ambient atmosphere in which the 4th process of the above contains nitrogen in the manufacture approach of a semiconductor device according to claim 19.

[Claim 26] It is the manufacture approach of the semiconductor device characterized by being carried out so that the 4th process of the above may introduce nitrogen also into the above-mentioned source field and a drain field in the manufacture approach of a semiconductor device according to claim 19, 20, 21, 22, 23, 24, or 25.

[Claim 27] In the manufacture approach of a semiconductor device according to claim 19, 20, 21, 22, 23, 24, or 25 The process which introduces the low-concentration 1st conductivity-type impurity in a semi-conductor substrate, and forms a low concentration source drain field by using the above-mentioned gate electrode as a mask before the 4th process of the above, The manufacture approach of the semiconductor device characterized by having further the process which forms an insulator sidewall on the both-sides side of the above-mentioned gate electrode before the 5th process of the backward above of the 4th process of the above.

[Claim 28] The manufacture approach of the semiconductor device characterized by having further the process which forms the low resistance film which contains a metal at least on the above-mentioned source field and a drain field after the 5th process of the above in the manufacture approach of a semiconductor device according to claim 19, 20, 21, 22, 23, 24, or 25.

[Claim 29] the manufacture approach of a semiconductor device according to claim 19, 20, 21, 22, 23, 24, 25, 26, 27, or 28 -- setting -- the 2nd process of the above -- the above -- a conductor -- a film top -- an insulator layer -- further -- depositing -- the 3rd process of the above -- the above -- a conductor -- the manufacture approach of the semiconductor device which carries out patterning of the film and an oxide film, simultaneously the above-mentioned insulator layer, and is characterized by forming a gate top insulator layer on the above-mentioned gate electrode.

[Claim 30] In the manufacture approach of a semiconductor device according to claim 19 at the 1st process of the above The isolation which surrounds the 2nd active region for forming the 1st active region for forming a nMIS mold

field-effect transistor and the above-mentioned pMIS mold field-effect transistor according to an individual is formed. The film is deposited. the 2nd process of the above -- the 1st and 2nd active-regions top of the above -- an oxide film and a conductor -- at the 3rd process of the above Patterning of the film is carried out. the above-mentioned oxide film and a conductor -- on the 1st and 2nd active regions of the above The gate oxide and the gate electrode of a nMIS mold and a pMIS mold field-effect transistor are formed, respectively. At the 4th process of the above Nitrogen is introduced into the edge by the side of a drain field at least among the both ends of the gate oxide of the above-mentioned nMIS mold field-effect transistor, and an acid nitrated case is formed. At the 5th process of the above The manufacture approach of the semiconductor device characterized by introducing the 1st and 2nd conductivity-type impurity into the field located in the method of both sides of the above-mentioned gate electrode among the 1st and 2nd active regions of the above, respectively, and forming the source field and drain field of the above-mentioned nMIS mold and a pMIS mold field-effect transistor.

[Claim 31] In the manufacture approach of a semiconductor device according to claim 30 before the 5th process of the backward above of the 3rd process of the above It has further the process which forms the mask member of a wrap 1st for the 2nd active region of the above. At the 4th process of the above The manufacture approach of the semiconductor device characterized by forming the above-mentioned acid nitrated case by pouring in nitrogen ion from a direction including the upper part on the active region of the above 1st, and the direction which inclined to the drain field side at least where the mask member of the above 1st is formed.

[Claim 32] In the manufacture approach of a semiconductor device according to claim 30 or 31, the process which forms the mask member of a wrap 2nd for the 1st active region of the above before the 5th process of the backward above of the 3rd process of the above, and where the mask member of the above 2nd is formed The manufacture approach of the semiconductor device characterized by having further the process which pours in nitrogen ion from an almost vertical direction into the active region of the above 2nd to the front face of the above-mentioned semi-conductor substrate.

[Claim 33] the manufacture approach of a semiconductor device according to claim 30, 31, or 32 -- setting -- the 2nd process of the above -- the above -- a conductor -- a film top -- an insulator layer -- further -- depositing -- the 3rd process of the above -- the above -- a conductor -- the manufacture approach of the

semiconductor device which carries out patterning of the film and an oxide film, simultaneously the above-mentioned insulator layer, and is characterized by forming a gate top insulator layer on the above-mentioned gate electrode in the above 1st and the 2nd active region.

[Claim 34] The 1st process which introduces the impurity for carrier generation and forms the 1st impurity diffused layer in the semiconductor region of a semi-conductor substrate, The 2nd process which introduces nitrogen and forms a nitrogen diffusion layer in the semiconductor region of the above-mentioned semi-conductor substrate so that the defect more than the detection level resulting from the collision with a semi-conductor atom may not be made to produce, The above-mentioned semi-conductor substrate is heated and it has the 3rd process which activates the above-mentioned impurity for carrier generation. The 1st process of the above, and the 2nd process the inside of both processes -- either -- previously -- and the manufacture approach of the semiconductor device characterized by carrying out so that the 1st impurity diffused layer of the above and the above-mentioned nitrogen diffusion layer may overlap at least.

[Claim 35] It is the manufacture approach of the semiconductor device characterized by being carried out by heat-treating the above-mentioned semi-conductor substrate in the gas ambient atmosphere in which the 1st process of the above contains nitrogen at least in the manufacture approach of a semiconductor device according to claim 34.

[Claim 36] It is the manufacture approach of the semiconductor device characterized by performing the 3rd process of the above in an ammonia gas ambient atmosphere in the manufacture approach of a semiconductor device according to claim 35.

[Claim 37] The 3rd process of the above is the manufacture approach of the semiconductor device characterized by performing temperature at 900 degrees or more, and performing time amount under the conditions for 10 or less seconds in the manufacture approach of a semiconductor device according to claim 36.

[Claim 38] It is the manufacture approach of the semiconductor device by which it is carrying-out by generating plasma in gas ambient atmosphere in which 1st process of the above contains nitrogen at least in manufacture approach of semiconductor device according to claim 34 characterized.

[Claim 39] The manufacture approach of the semiconductor device characterized by having further the process which forms the silicide film on the above-mentioned source field and a drain

field after the 3rd process of the above in the manufacture approach of a semiconductor device according to claim 34.

[Claim 40] In the manufacture approach of a semiconductor device according to claim 34, 35, 36, 37, or 38 in the above-mentioned semi-conductor substrate The MIS mold field-effect transistor formation field is prepared, and it has further the process which forms gate dielectric film and a gate electrode on the above-mentioned MIS mold field-effect transistor formation field. At the 1st process of the above, after forming the above-mentioned gate dielectric film and a gate electrode The manufacture approach of the semiconductor device characterized by introducing the above-mentioned impurity for carrier generation into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned MIS mold field-effect transistor formation fields, and forming the source field and drain field of the above-mentioned MIS mold field-effect transistor in it.

[Claim 41] It is the manufacture approach of the semiconductor device characterized by to form the gate dielectric film which consists of an oxide film, and to perform the 2nd process of the above after the process which forms the above-mentioned gate dielectric film and a gate electrode, and to introduce nitrogen also into the both ends of the above-mentioned gate dielectric film at the 2nd process of the above, and to form an acid nitrated case in the manufacture approach of a semiconductor device according to claim 40 at the process which forms the above-mentioned gate dielectric film and a gate electrode.

[Claim 42] In the manufacture approach of a semiconductor device according to claim 40, after the process which forms the above-mentioned gate dielectric film and a gate electrode, and before the 1st process of the above The process which introduces the 2nd impurity for carrier generation of the low-concentration and same conductivity type, and forms an extension field in the above-mentioned MIS mold field-effect transistor formation field rather than the above-mentioned impurity for carrier generation introduced into the above-mentioned source field and the drain field, It has further the process which forms an insulator sidewall on the both-sides side of the above-mentioned gate electrode. At the 1st process of the above The above-mentioned impurity for carrier generation is introduced in the field located in the method of both sides of the above-mentioned gate electrode and a sidewall among the above-mentioned MIS mold field-effect transistor formation fields. At the 2nd process of the above The manufacture approach of the semiconductor device

characterized by forming the above-mentioned nitrogen diffusion layer so that a part of above-mentioned extension field [at least] may be included.

[Claim 43] The manufacture approach of the semiconductor device characterized by to have further the process which introduces the 3rd impurity of low concentration and a reverse conductivity type for carrier generation, and forms a pocket field in the above-mentioned MIS mold field-effect transistor formation field in the manufacture approach of a semiconductor device according to claim 42 rather than the above-mentioned impurity for carrier generation which introduced into the above-mentioned source field and a drain field after the process which forms the above-mentioned gate dielectric film and a gate electrode, and before the 1st process of the above.

[Claim 44] It is the manufacture approach of the semiconductor device characterized by carrying out before the process and the 1st process of the above that the 2nd process of the above forms the above-mentioned gate dielectric film and a gate electrode in the manufacture approach of a semiconductor device according to claim 40, 42, or 43, covering the whole longitudinal direction of the above-mentioned MIS mold field-effect transistor formation field, and forming a nitrogen diffusion layer.

[Claim 45] The manufacture approach of the semiconductor device characterized by having further the process which forms the silicide film on the above-mentioned source field, a drain field, and a gate electrode after the 3rd process of the above in the manufacture approach of a semiconductor device according to claim 40, 41, 42, 43, or 44.

[Claim 46] In the manufacture approach of a semiconductor device according to claim 34, 35, 36, 37, or 38 in the above-mentioned semi-conductor substrate The process which the bipolar transistor formation field is prepared, introduces the 1st conductivity-type impurity into the above-mentioned bipolar transistor formation field, and forms the collector field of a bipolar transistor, It has further the process which introduces the 2nd conductivity-type impurity and forms the base region of a bipolar transistor in the above-mentioned collector field. At the 1st process of the above The manufacture approach of the semiconductor device which introduces the 1st conductivity-type impurity, forms the emitter region of the above-mentioned bipolar transistor in the above-mentioned base region, and is characterized by introducing nitrogen into a field including a part of above-mentioned emitter region [at least] at the 2nd process of the above.

[Claim 47] In the manufacture approach of a semiconductor device according to

claim 34, 35, 36, 37, or 38 in the above-mentioned semi-conductor substrate The process which the bipolar transistor formation field is prepared, introduces the 1st conductivity-type impurity into the above-mentioned bipolar transistor formation field, and forms the collector field of a bipolar transistor, It has further the process which introduces the 1st conductivity-type impurity in the above-mentioned collector field, and forms the emitter region of the above-mentioned bipolar transistor after the 1st process of the above. At the 1st process of the above The manufacture approach of the semiconductor device characterized by introducing a 2nd conductivity-type pure object into the field which encloses the inside of the above-mentioned collector field, and the above-mentioned emitter region, forming the base region of a bipolar transistor and introducing nitrogen into the field which includes a part of above-mentioned base region [at least] at the 2nd process of the above.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device which carried the MIS mold field-effect transistor and the bipolar transistor, and its manufacture approach, especially relates to the engine performance of the semiconductor device by improvement of the structure of an impurity diffused layer or gate dielectric film, and the cure against improvement of dependability.

[0002]

[Description of the Prior Art] In the MIS mold field-effect transistor which prepares a gate electrode through gate oxide on a semi-conductor substrate, and comes to prepare an impurity diffusion field (source drain field) in the both sides of a gate electrode conventionally, the role of gate oxide is very important. In the semiconductor device with which low-battery-izing of detailed-izing of a component and driver voltage and improvement in the speed of operation are especially demanded like recently, in order to meet these demands, maintaining high dependability, a various and advanced device is required also about the structure of not only physical dimensions, such as thickness of gate oxide, but gate oxide.

[0003] Degradation of the function of gate oxide according to the hot carrier of a nMOS mold transistor especially in a CMOS device (fluctuation of a threshold electrical potential difference) is controlled to one of the techniques which reform the structure of such gate oxide,

and the technique which forms an acid nitrated case into gate oxide is in it that improvement in dependability should be realized. For example, nitrogen ion is poured in into a gate electrode and a semi-conductor substrate after formation of a gate electrode, and he diffuses this nitrogen by next heat treatment within a gate electrode, and is trying to make an acid nitrated case form into gate oxide by 1993, IEEE, and the approach shown in IEDM93 digest P325-328. Hereafter, the process which forms an acid nitrated case using this approach is explained concretely, referring to a drawing.

[0004] First, at the process shown in drawing 22 (a), isolation 4 is formed in a part of silicon substrate 1, after forming an oxide film and depositing the polish recon film further on the silicon substrate 1 in the active region surrounded by isolation 4, patterning of an oxide film and the polish recon film is carried out according to photolithography and a dry etching process, and gate oxide 2 and the gate electrode 3 are formed.

[0005] Next, at the process shown in drawing 22 (b), the nitrogen diffusion layer 6 is formed in the field near the front face in a silicon substrate 1 at the same time it diffuses nitrogen ion by heat treatment and forms the acid nitrated case 5 into gate oxide 2, after pouring in nitrogen ion (N+) from the upper part of a substrate into the silicon substrate 1 in the gate electrode 3 and an active region.

[0006] Next, at the process shown in drawing 22 (c), low-concentration arsenic ion (As+) is mostly poured in from a perpendicular direction, and n mold low concentration source drain field 7 is formed in the field near the front face in a silicon substrate 1.

[0007] Next, at the process shown in drawing 22 (d), after depositing thicker silicon oxide on a substrate, etchback is performed, after forming a sidewall 8 on the both-sides side of the gate electrode 3, impregnation of high-concentration arsenic ion (As+) is performed further mostly from a perpendicular direction, and n mold high concentration source drain field 9 is formed in a way outside the above-mentioned n mold low concentration source drain field 7.

[0008] However, as structure of the whole CMOS device, n mold impurity (arsenic) is doped in the gate electrode of a nMOS mold field-effect transistor, p mold impurity (boron) is doped in the gate electrode of a pMOS mold field-effect transistor, and the so-called dual gate type of structure is taken..

[0009] In this condition, the nMOS mold field-effect transistor which has the so-called LDD structure suitable for low-battery[detailed-izing and]-izing and high-speed operation-ization can be formed on a silicon substrate 1. And he is trying to control hot carrier degradation by forming the acid nitrated case 5 in the gate oxide 2 of a transistor. It is shown in

it that hot carrier degradation can be controlled, so that this reference has many injection rates of nitrogen ion, and in the nMOS mold field-effect transistor from which degradation (lifting of a threshold etc.) of the property especially by the hot electron poses a problem, the effectiveness is large.

[0010] In addition, the effectiveness prevented by the acid nitrated case in gate oxide is acquired [boron running to the surface channel field in a substrate, and having an adverse effect on the property of a transistor at a pMOS mold field-effect transistor side, and].

[0011]

[Problem(s) to be Solved by the Invention] However, formation of the acid nitrated case 5 as shown in drawing 22 (d) like the conventional approach observed the phenomenon in which the engine performance of a transistor -- the driving force of a transistor declines on the contrary -- deteriorated. The cause becomes excessive [the diffusion depressant action of impurities such as arsenic in the gate electrode 3 by the acid nitrated case 5, and boron,], and is conjectured for it to become impossible to demonstrate the advantage of dual gate structure, and to be in causing buildup of resistance by depletion-izing of a gate electrode etc. Moreover, although the cause is unknown if an acid nitrated case is formed into the gate oxide of a pMOS mold field-effect transistor, it is also reported that the mutual conductance of a transistor decreases.

[0012] On the other hand, there are the following problems on the property of the diffusion layer of a transistor as a problem other than the above-mentioned problem.

[0013] consuming the silicon which is a diffusion layer, in case silicide is formed in improvement in the speed of an MOS device, and high integration in the Salicide (Self-align-silicidation) process which is the typical technique of the reduction in resistance of the indispensable gate and a source drain diffusion layer -- taking into consideration -- stable -- low -- if it is going to form the silicide film [****] thickly, shallow junction formation will become difficult. Moreover, since the high impurity concentration of a silicide interface also falls and parasitism resistance becomes high, a drain current falls.

[0014] Although it becomes remarkable [the above-mentioned problem] when pouring in BF2 (boron flora IDO boron fruoride) ion in surface channel mold p-MOSFET and forming p mold diffusion layer especially, the in that case still more nearly following new technical problems arise. Drawing 23 is BF2 in a silicon substrate. Although B (BORON boron) ion was poured in on condition that acceleration energy 10keV and dose 2x1015cm-2, the boron SIMS profile after

carrying out heat-of-activation processing of each the condition for 1000 degrees C and 10 seconds is indicated to be what poured in ion on condition that acceleration energy 30keV and dose 2x1015cm-2.

[0015] First, BF2 In impregnation, in order that fluorine and boron may join together, two peaks of the concentration of a lifting and an impurity exist deviation (refer to drawing 23). Although the peak especially with high concentration exists in the substrate front-face side, since this boron exists in the field silicide-ized behind, it will not contribute to formation of a final diffusion layer, but will become the concentration which fell from the peak of the concentration to which the diffusion layer must originally also have had the concentration of the interface of silicide and a diffusion layer as a result, and contact resistance of this part will increase. Furthermore, since an impurity is simultaneously introduced also in a gate electrode in case an impurity is introduced to a diffusion layer in the case of a surface channel mold transistor, from a gate electrode, an impurity will fall out, it oozes out to a substrate side through gate dielectric film, (penetration), and a phenomenon must also pay attention.

[0016] Next, drawing 24 is BF2. The Quasi-staticC-V property of impregnation (30keV, 2x1015cm-2) and B impregnation (10keV, 2x1015cm-2) is shown. Usually, he is BF2, although a stain broth has not happened and wave-like flat band voltage is 0.86V. It turns out that it shifts a little in impregnation, and has become 0.88V, and the stain broth has arisen a little.

[0017] Drawing 25 is the boron and BF2 of flat band voltage. It is drawing showing an impregnation dose dependency. BF2 In impregnation, with the increment in acceleration energy or a dose, the shift of flat band voltage also becomes large and a stain broth becomes remarkable. These things to BF2 Since it leads to taking the means which enlarge the acceleration energy and the dose in the case of impurity impregnation in order to make high high impurity concentration in the interface of the silicide after silicide formation and a diffusion layer in impregnation promoting the stain broth of the impurity from a gate electrode to a substrate, it is becoming difficult to form a powerful transistor.

[0018] The explanation about an above-mentioned trouble is BF2. In impregnation, followed, but while -- ** it is the stain of the boron from a gate electrode to a substrate in B impregnation -- alike -- receiving -- BF2 Although nonconformity is eased rather than the case of impregnation (refer to [drawing 24 and] the drawing 2525), as shown in drawing 13 Since the pn junction section between a source drain field and a substrate field is formed in a

deep part, the application to a detailed device is difficult.

[0019] The 1st object of this invention is shown in aiming at offer of a highly efficient and reliable semiconductor device and its manufacture approach by improving the structure of the acid nitrated case in gate oxide.

[0020] Moreover, the 2nd object of this invention is related with the semiconductor device which needs shallow junction formation. Without making property degradation and cost increase, control diffusion and shallow junction is formed. In realizing both the salicide process which is to realize the detailed device of high performance and silicide-izes a diffusion layer especially, and the dual gate which has p-MOSFET of a surface channel mold the stain broth of boron even with ** And it is in forming the silicide film of low resistance and forming shallow junction.

[0021]

[Means for Solving the Problem] The means which this invention provided in order to attain the 1st object of the above is by [of gate oxide] preparing an acid nitrated case in the drain side edge section at least to prevent control of hot carrier degradation, and the performance degradation by depletion-izing of the gate etc. Specifically, the means about the 1st semiconductor device indicated by claims 1-8 and the means about the manufacture approach of the 1st semiconductor device indicated by claims 18-32 are provided.

[0022] The means which this invention provided in order to attain the 2nd object of the above is by introducing nitrogen in the condition of not making an impurity diffused layer producing the defect more than the detection level resulting from the collision with nitrogen and a semi-conductor atom to improve the concentration profile of an impurity diffused layer, preventing degradation of the property by the defect. Specifically, the means about the 2nd semiconductor device indicated by claims 9-18 and the means about the manufacture approach of the 2nd semiconductor device indicated by claims 34-47 are provided.

[0023] In the semiconductor device which carried the MIS mold field-effect transistor on the semi-conductor substrate as the 1st semiconductor device of this invention was indicated by claim 1 The active region where the above-mentioned MIS mold field-effect transistor was formed in some above-mentioned semi-conductor substrates, The gate oxide formed on the above-mentioned active region, and the gate electrode formed on the above-mentioned gate oxide, It has the source field and drain field which introduced the impurity into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and

were formed in it, and the acid nitrated case formed in the edge by the side of the above-mentioned drain field at least among the both ends of the above-mentioned gate oxide.

[0024] Thereby, since the acid nitrated case is formed only in the edge of gate oxide, degradation of the engine performance of the transistor resulting from that the diffusion to the lower part of the impurity in a gate electrode is barred, depletion-ization of a gate electrode, etc. is prevented. On the other hand, although it becomes a cause that a hot carrier is captured by the gate dielectric film by the side of a drain, since the acid nitrated case is effectively formed to the gate oxide by the side of the drain leading to degradation in this way, hot carrier degradation can improve hot carrier dependability.

[0025] In claim 1, it is desirable to form the above-mentioned acid nitrated case in the both ends of the above-mentioned gate oxide as indicated by claim 2.

[0026] Thereby, the control function of hot carrier degradation is obtained more certainly.

[0027] In claim 1, it can have further the nitrogen diffusion layer formed in a part of drain field at least among the above-mentioned source field and the drain field as indicated by claim 3.

[0028] Since the channeling at the time of an ion implantation is prevented by this according to the nitrogen diffusion layer formed in a semi-conductor substrate, it becomes the structure which is stabilized and can form a source field and a drain field, and the property of a transistor is stabilized.

[0029] In claim 2, the above-mentioned nitrogen diffusion layer can be formed more shallowly than the above-mentioned source field and a drain field as indicated by claim 4.

[0030] Thereby, since the high impurity concentration especially in the field near a front face in a semi-conductor substrate becomes high, sheet resistance can be reduced.

[0031] In claim 1, it has a nMIS mold field-effect transistor and a pMIS mold field-effect transistor on a semi-conductor substrate as indicated by claim 5. The active region where the above-mentioned MIS mold field-effect transistor was used as the above-mentioned nMIS mold field-effect transistor, and the above-mentioned pMIS mold field-effect transistor was formed in some above-mentioned semi-conductor substrates, The gate oxide formed on the above-mentioned active region, and the gate electrode formed on the above-mentioned gate oxide, It shall have the source field and drain field which introduced the impurity into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and were formed in it, and the acid nitrated

case shall not be formed in the gate oxide of the above-mentioned pMIS mold field-effect transistor.

[0032] Thereby, in a nMIS mold field-effect transistor, the same operation as an operation of above-mentioned claim 1 is done so. On the other hand, in a pMIS mold field-effect transistor, since the acid nitrated case is not formed in gate oxide, lowering of a mutual conductance is avoidable.

[0033] In claim 5, the above-mentioned nMIS mold field-effect transistor can be further equipped with the nitrogen diffusion layer formed at least in the part in the above-mentioned source field and a drain field as indicated by claim 6.

[0034] The operation same thereby respectively as claims 2 and 3 is done so.

[0035] In claim 6, the above-mentioned nitrogen diffusion layer can be formed more shallowly than any of the above-mentioned source field and a drain field as indicated by claim 7.

[0036] Thereby, the same operation as claim 4 is done so.

[0037] In claims 1, 2, 3, 4, 5, and 6 or 7, it can have further the gate top insulator layer by which patterning was carried out to the above-mentioned gate electrode and coincidence on the above-mentioned gate electrode as indicated by claim 8.

[0038] Since the gate electrode top has structure protected by the insulator layer in case nitrogen is introduced into the edge of gate oxide by the ion implantation and thermal diffusion of an impurity, plasma nitriding, etc. and an acid nitrated case is formed by this, it becomes possible to prevent certainly degradation of the engine performance of the transistor resulting from depletion-ization of a gate electrode etc.

[0039] The 2nd semiconductor device of this invention is equipped with the nitrogen diffusion layer containing the nitrogen introduced into the semi-conductor substrate, the impurity diffused layer which is formed in the above-mentioned semi-conductor substrate, and contains the 1st conductivity-type impurity for carrier generation, and the field containing a part of above-mentioned impurity diffused layer [at least] in the condition that the defect resulting from the collision with a semi-conductor atom does not exceed detection level as indicated by claim 9.

[0040] Since diffusion of the 1st conductivity-type impurity in an impurity diffused layer is controlled by existence of nitrogen, this will concentrate the field where the concentration of the 1st conductivity-type impurity is high on the field near the front face of a semi-conductor substrate in in an impurity diffused layer. Therefore, the sheet resistance of an impurity diffused layer becomes very small, and can obtain various kinds of semiconductor devices which were

excellent in the property using the impurity diffused layer which has such small sheet resistance. And since there are very few defects in an impurity diffused layer, the adverse effect which it has on the property of a semiconductor device is also avoided.

[0041] While it sets to claim 9 and the concentration of the above-mentioned 1st conductivity-type impurity in the above-mentioned impurity diffused layer decreases toward the method of the back of the above-mentioned semi-conductor substrate from the maximum concentration location of the field near the front face in a semi-conductor substrate as indicated by claim 10 It is large until the reduction rate arrives at the predetermined location of the lower part which passed through the above-mentioned maximum concentration location, and in the field which goes to the method of the back rather than the above-mentioned predetermined location, it is desirable to constitute as it has the distribution to which a reduction rate becomes small.

[0042] By this, the concentration profile of the 1st conductivity-type impurity becomes ideal in in an impurity diffused layer, and the operation effectiveness of claim 1 will be notably done so.

[0043] In claim 9 or 10, it shall have further the silicide film formed on the above-mentioned impurity diffused layer, and the maximum concentration location of the above-mentioned 1st conductivity-type impurity in the above-mentioned impurity diffused layer shall be in the method of directly under of an interface with the above-mentioned silicide film as indicated by claim 11.

[0044] Thereby, he is BF2. Since it is in the place into which the peak of concentration went [like] for a while not from near directly under [on the front face of a substrate] but from the substrate front face when impregnation restricts diffusion, when the silicide film is formed, the peak location of concentration will exist in the method of directly under of the silicide film. Therefore, junction leak will also be reduced while the sheet resistance of an impurity diffused layer becomes very small.

[0045] The gate dielectric film formed on the active region in a semi-conductor substrate in the above-mentioned semiconductor device in claim 9 or 10 as indicated by claim 12, The source field and drain field which are formed in the gate electrode formed on this gate dielectric film, and the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and contain the 1st conductivity-type impurity, It considers as the MIS mold field-effect transistor which has the channel field which is formed between the above-mentioned source field and a

drain field among the above-mentioned active regions, and contains the 2nd conductivity-type impurity. the above-mentioned nitrogen diffusion layer can be formed in a field including the above-mentioned source field and a part of each drain field [at least].

[0046] The semiconductor device which has the small source drain field of sheet resistance by this is obtained.

[0047] The sidewall which consists of an insulating ingredient formed on the both-sides side of the above-mentioned gate electrode in claim 12 as indicated by claim 13, It has further the extension field which is formed, respectively between the above-mentioned source field and a drain field, and the direct lower part field of the above-mentioned gate electrode, and contains the low-concentration 1st conductivity-type impurity rather than the above-mentioned source field and a drain field. The above-mentioned nitrogen diffusion layer can be continued and formed also in the above-mentioned extension field.

[0048] In claim 12 or 13, the above-mentioned nitrogen diffusion layer may also be covering the above-mentioned channel field as indicated by claim 14.

[0049] By claim 12 or 13, since a pn junction part becomes shallow in a channel field, channel resistance can be reduced.

[0050] the thing which enter into the above-mentioned channel field side to the case where there be no above-mentioned nitrogen , in the field near the front face in the above-mentioned semi-conductor substrate and which constitute from a method of the back on the other hand so that it may keep away from a channel field side be desirable in claim 12 in the part in which the concentration of the above-mentioned impurity for carrier generation adjoin the above-mentioned channel field in the field beyond a predetermined value among the above-mentioned source field and a drain field as indicate by claim 15 .

[0051] Parasitic capacitance also becomes small, while parasitism resistance of a transistor becomes small, the resistance over a punch through becomes large by this and the control function of a short channel effect improves. That is, the structure to which working speed was highly suitable for detailed-ization will be acquired.

[0052] In claims 12, 13, and 14 or 15, it shall have further the silicide film formed on the above-mentioned source field and the above-mentioned drain field, and the maximum concentration location of the above-mentioned impurity for carrier generation in the field in which the above-mentioned nitrogen diffusion layer was formed among the above-mentioned source field and the drain field shall be near an interface with the

above-mentioned silicide film as indicated by claim 16.

[0053] Thereby, the small MIS mold field-effect transistor of junction leak with the small and sheet resistance in a source drain field is obtained.

[0054] The emitter region which is formed in a part of active region in the above-mentioned semi-conductor substrate in the above-mentioned semiconductor device, and contains the 2nd conductivity-type impurity in claim 9 as indicated by claim 17, The base region which is formed so that the above-mentioned emitter region may be surrounded in the above-mentioned active region, and contains the 1st conductivity-type impurity, It can consider as the bipolar transistor which has the collector field which is formed in the field which contains the lower part of the above-mentioned base region in the above-mentioned active region, and contains the 2nd conductivity-type impurity, and the above-mentioned nitrogen diffusion layer can be formed in a field including a part of above-mentioned emitter region [at least].

[0055] Since the field where the high impurity concentration in an emitter region is high concentrates near the front face of a semi-conductor substrate by this, resistance of an emitter region becomes small and a bipolar transistor with a high current amplification factor is obtained.

[0056] The emitter region which is formed in a part of active region in the above-mentioned semi-conductor substrate in the above-mentioned semiconductor device, and contains the 2nd conductivity-type impurity in claim 9 as indicated by claim 18, The base region which is formed so that the above-mentioned emitter region may be surrounded in the above-mentioned active region, and contains the 1st conductivity-type impurity, It can consider as the bipolar transistor which has the collector field which is formed in the field which contains the lower part of the above-mentioned base region in the above-mentioned active region, and contains the 2nd conductivity-type impurity, and the above-mentioned nitrogen diffusion layer can be formed in a field including a part of above-mentioned base region [at least].

[0057] Since the impurity atom concentration profile in a base region becomes steep by this and the thickness of a base region becomes small, base resistance is reduced and the bipolar transistor which has high cut-off frequency is obtained.

[0058] The manufacture approach of the 1st semiconductor device concerning this invention In the manufacture approach of a semiconductor device of having carried the MIS mold field-effect transistor as indicated by claim 19 the 1st process which forms the isolation surrounding an

active region on a semi-conductor substrate, and the above-mentioned active-region top -- an oxide film and a conductor -- with the 2nd process which deposits the film the above-mentioned oxide film and a conductor -- patterning of the film being carried out and with the 3rd process which forms the gate oxide and the gate electrode of the above-mentioned MIS mold field-effect transistor, respectively The 4th process which introduces nitrogen into the edge by the side of a drain field at least among the both ends of the above-mentioned gate oxide, and forms an acid nitrated case, It has the 5th process which introduces the 1st conductivity-type impurity into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned active regions, and forms the source field and drain field of the above-mentioned MIS mold field-effect transistor in it.

[0059] By this approach, the semiconductor device which has the configuration of claim 1 is obtained.

[0060] In claim 19, the 4th process of the above can form the above-mentioned acid nitrated case by pouring in nitrogen ion from a direction including the direction which carried out before the 5th process of the backward above of the 3rd process of the above, and inclined to the drain field side at least with large inclination ion-implantation from the upper part of the above-mentioned gate oxide and a gate electrode as indicated by claim 20.

[0061] By this approach, since nitrogen ion is poured in by the large inclination, an acid nitrated case is formed only in the edge of gate oxide. Since sufficient acid nitrated case to control hot carrier degradation can be formed even if it makes concentration of nitrogen ion thin weakly [energy / impregnation] compared with pouring nitrogen ion into the whole gate electrode in that case, depletion-ization of a gate electrode is not caused. Moreover, since the nitrogen volume poured in into a semi-conductor substrate decreases, the crystalline turbulence in an active region is also reduced as much as possible. Therefore, a reliable transistor with the good engine performance will be formed.

[0062] In claim 20, impurity ion can be poured in at the 4th process of the above from at least two or more directions including the direction leaning to the above-mentioned drain side, and the direction leaning to the above-mentioned source field side as indicated by claim 21.

[0063] By this approach, since an acid nitrated case is formed in the both ends of gate oxide, fewer transistors of hot carrier degradation are formed.

[0064] In claim 20 or 21, impurity ion can be poured in at the 4th process of the above from the direction to which 10 degrees or more inclined to the direction vertical to the front face of the

above-mentioned semi-conductor substrate in the cross section parallel to the direction of a channel of the above-mentioned transistor as indicated by claim 22.

[0065] By this approach, an acid nitrated case can be certainly formed in the edge of gate oxide.

[0066] In claim 19, it can carry out by heat-treating the above-mentioned semi-conductor substrate in the gas ambient atmosphere which includes the 4th process of the above for nitrogen at least as indicated by claim 23.

[0067] In claim 23, the 4th process of the above can be performed in an ammonia gas ambient atmosphere as indicated by claim 24.

[0068] In claim 19, it can carry out by generating the plasma in the gas ambient atmosphere which includes the 4th process of the above for nitrogen as indicated by claim 25.

[0069] The same effectiveness as claim 19 can be acquired also by the approach of claims 23-25.

[0070] In claims 19, 20, 21, 22, 23, and 24 or 25, the 4th process of the above can be performed so that nitrogen may be introduced also into the above-mentioned source field and a drain field, as indicated by claim 26.

[0071] By this approach, the transistor which has the small source drain field of sheet resistance will be formed.

[0072] It sets to claims 19, 20, 21, 22, 23, and 24 or 25 as indicated by claim 27. The process which introduces the low-concentration 1st conductivity-type impurity in a semi-conductor substrate, and forms a low concentration source drain field by using the above-mentioned gate electrode as a mask before the 4th process of the above, Before the 5th process of the backward above of the 4th process of the above, it can have further the process which forms an insulator sidewall on the both-sides side of the above-mentioned gate electrode.

[0073] The transistor which has LDD structure and has the small source drain field of sheet resistance by this approach will be formed.

[0074] In claims 19, 20, 21, 22, 23, and 24 or 25, it can have further the process which forms the low resistance film which contains a metal at least on the above-mentioned source field and a drain field after the 5th process of the above as indicated by claim 28.

[0075] By this approach, the transistor to which sheet resistance has a very small source drain field will be formed.

[0076] it is indicated by claim 29 -- as -- claims 19, 20, 21, 22, 23, 24, 25, 26, and 27 or 28 -- setting -- the 2nd process of the above -- the above -- a conductor -- a film top -- an insulator layer -- further -- depositing -- the 3rd process of the above -- the above -- a conductor -- patterning of the film and an oxide film, simultaneously the above-mentioned

insulator layer can be carried out, and a gate top insulator layer can be formed on the above-mentioned gate electrode.

[0077] By this approach, since the amount of installation of the nitrogen into a gate electrode can be controlled, lowering of the driving force of the transistor resulting from depletion-ization of a gate electrode can be prevented certainly.

[0078] It sets to claim 19 as indicated by claim 30. At the 1st process of the above The isolation which surrounds the 2nd active region for forming the 1st active region for forming a nMIS mold field-effect transistor and the above-mentioned pMIS mold field-effect transistor according to an individual is formed. The film is deposited. the 2nd process of the above -- the 1st and 2nd active-regions top of the above -- an oxide film and a conductor -- at the 3rd process of the above Patterning of the film is carried out. the above-mentioned oxide film and a conductor -- on the 1st and 2nd active regions of the above The gate oxide and the gate electrode of a nMIS mold and a pMIS mold field-effect transistor are formed, respectively. At the 4th process of the above Nitrogen is introduced into the edge by the side of a drain field at least among the both ends of the gate oxide of the above-mentioned nMIS mold field-effect transistor, and an acid nitrated case is formed. At the 5th process of the above The 1st and 2nd conductivity-type impurity can be introduced into the field located in the method of both sides of the above-mentioned gate electrode among the 1st and 2nd active regions of the above, respectively, and the source field and drain field of the above-mentioned nMIS mold and a pMIS mold field-effect transistor can be formed.

[0079] By this approach, a reliable nMIS mold field-effect transistor with the good engine performance is manufactured in the 1st active region. On the other hand, in the 2nd active region, a pMIS mold field-effect transistor with a good mutual-conductance property will be formed by not forming an acid nitrated case.

[0080] It sets to claim 30 as indicated by claim 31. Before the 5th process of the backward above of the 3rd process of the above It has further the process which forms the mask member of a wrap 1st for the 2nd active region of the above. At the 4th process of the above The above-mentioned acid nitrated case can be formed by pouring in nitrogen ion from the direction which inclined to the drain field side at least with large inclination ion-implantation from the upper part of the above-mentioned gate oxide on the active region of the above 1st, and a gate electrode, where the above-mentioned mask member is formed.

[0081] By this approach, a nMIS mold field-effect transistor with the reliable

good engine performance is manufactured easily.

[0082] The process which forms the mask member of a wrap 2nd for the 1st active region of the above before the 5th process of the backward above of the 3rd process of the above, and where the mask member of the above 2nd is formed, in claim 30 or 31, as indicated by claim 32 It can have further the process which pours in nitrogen ion from an almost vertical direction into the active region of the above 2nd to the front face of the above-mentioned semi-conductor substrate.

[0083] By this approach, since a nitrogen diffusion layer is formed in the 2nd active region, the channeling of the impurity ion in the case of the source field in the 5th process and a drain field is prevented, and formation of a source field and a drain field is stabilized.

[0084] it is indicated by claim 33 -- as -- claims 30 and 31 or 32 -- setting -- the 2nd process of the above -- the above -- a conductor -- a film top -- an insulator layer -- further -- depositing -- the 3rd process of the above -- the above -- a conductor -- patterning of the film and an oxide film, simultaneously the above-mentioned insulator layer can be carried out, and a gate top insulator layer can be formed on the above-mentioned gate electrode in the above 1st and the 2nd active region.

[0085] By this approach, the large CMOS mold field-effect transistor of the small driving force of depletion-izing of a gate electrode will be formed.

[0086] The manufacture approach of the 2nd semiconductor device of this invention as indicated by claim 34 The 1st process which introduces the impurity for carrier generation and forms the 1st impurity diffused layer in the semiconductor region of a semi-conductor substrate, The 2nd process which introduces nitrogen and forms a nitrogen diffusion layer in the semiconductor region of the above-mentioned semi-conductor substrate so that the defect more than the detection level resulting from the collision with a semi-conductor atom may not be made to produce, It has the 2nd process and the 3rd process which the above-mentioned semi-conductor substrate is heated [process] and activates the above-mentioned impurity for carrier generation. The 1st process of the above, and the 2nd process the inside of both processes -- either -- previously -- and it is the approach of performing so that the 1st impurity diffused layer of the above and the above-mentioned nitrogen diffusion layer may overlap at least.

[0087] By this approach, the semiconductor device which does an operation of claim 9 so will be formed easily. However, the 2nd process and 3rd process can be performed continuously.

[0088] In claim 34, it can carry out by

heat-treating the above-mentioned semi-conductor substrate in the gas ambient atmosphere which includes the 1st process of the above for nitrogen at least as indicated by claim 35.

[0089] Since the defect which originates in the collision with nitrogen ion like [in the case of pouring in nitrogen ion into a nitrogen diffusion layer] and a semi-conductor atom by this approach does not arise, a semiconductor device without degradation of the property resulting from a defect is obtained.

[0090] In claim 35, the 3rd process of the above can be performed in an ammonia gas ambient atmosphere as indicated by claim 36.

[0091] By this approach, since the introductory function of the nitrogen into a semi-conductor substrate becomes high especially, a nitrogen diffusion layer can be formed easily and promptly.

[0092] In claim 36, it is desirable that temperature performs at 900 degrees or more, and time amount performs the 3rd process of the above under the conditions for 10 or less seconds as indicated by claim 37.

[0093] In claim 34, it can carry out by generating the plasma in the gas ambient atmosphere which includes the 1st process of the above for nitrogen at least as indicated by claim 38.

[0094] Also by this approach, a nitrogen diffusion layer can be formed in the condition that there is almost no defect.

[0095] In claim 34, it can have further the process which forms the silicide film on the above-mentioned source field and a drain field after the 3rd process of the above as indicated by claim 39.

[0096] It sets to claims 34, 35, 36, and 37 or 38 as indicated by claim 40. In the above-mentioned semi-conductor substrate, an MIS mold field-effect transistor formation field is prepared. It has further the process which forms gate dielectric film and a gate electrode on the above-mentioned MIS mold field-effect transistor formation field. At the 1st process of the above After forming the above-mentioned gate dielectric film and a gate electrode The above-mentioned impurity for carrier generation can be introduced into the field located in the method of both sides of the above-mentioned gate electrode among the above-mentioned MIS mold field-effect transistor formation fields, and the source field and drain field of the above-mentioned MIS mold field-effect transistor can be formed in it.

[0097] This approach. The MIS mold field-effect transistor which has the small source drain field of sheet resistance can be formed.

[0098] In claim 40, at the process which forms the above-mentioned gate dielectric film and a gate electrode, the 2nd process of the above can be performed by forming the gate dielectric film which consists of an oxide film after the process which

forms the above-mentioned gate dielectric film and a gate electrode, and nitrogen can be introduced also into the both ends of the above-mentioned gate dielectric film at the 2nd process of the above, and an acid nitrated case can be formed as indicated by claim 41.

[0099] By this approach, sheet resistance can obtain a small transistor with large hot carrier resistance.

[0100] In claim 40, after the process which forms the above-mentioned gate dielectric film and a gate electrode, and before the 1st process of the above as indicated by claim 42 The process which introduces the 2nd impurity for carrier generation of the low-concentration and same conductivity type, and forms an extension field in the above-mentioned MIS mold field-effect transistor formation field rather than the above-mentioned impurity for carrier generation introduced into the above-mentioned source field and the drain field, It has further the process which forms an insulator sidewall on the both-sides side of the above-mentioned gate electrode. At the 1st process of the above The above-mentioned impurity for carrier generation is introduced in the field located in the method of both sides of the above-mentioned gate electrode and a sidewall among the above-mentioned MIS mold field-effect transistor formation fields. At the 2nd process of the above The above-mentioned nitrogen diffusion layer can be formed so that a part of above-mentioned extension field [at least] may be included.

[0101] By this approach, it has LDD structure and the small transistor of channel resistance will be formed.

[0102] It can have further the process which introduces the 3rd impurity for carrier generation of low concentration and a reverse conductivity type, and forms a pocket field in the above-mentioned MIS mold field-effect transistor formation field rather than the above-mentioned impurity for carrier generation introduced into the above-mentioned source field and the drain field after the process which forms the above-mentioned gate dielectric film and a gate electrode, and before the 1st process of the above in claim 42 as indicated by claim 43.

[0103] By this approach, the very high transistor of a short-channel-effect control function can be formed.

[0104] In claims 40 and 42 or 43, the 2nd process of the above can be performed before the process which forms the above-mentioned gate dielectric film and a gate electrode, and the 1st process of the above, can cover the whole longitudinal direction of the above-mentioned MIS mold field-effect transistor formation field, and can form a nitrogen diffusion layer as indicated by claim 44.

[0105] By this approach, a transistor with very small channel resistance will be obtained.

[0106] In claims 40, 41, 42, and 43 or 44, it can have further the process which forms the silicide film after the 3rd process of the above on the above-mentioned source field, a drain field, and a gate electrode as indicated by claim 45.

[0107] By this approach, it sets to claims 34, 35, 36, and 37 or 38 as indicated by claim 46. The process which prepares a bipolar transistor formation field, introduces the 1st conductivity-type impurity into the above-mentioned bipolar transistor formation field, and forms the collector field of a bipolar transistor in the above-mentioned semi-conductor substrate, It has further the process which introduces the 2nd conductivity-type impurity and forms the base region of a bipolar transistor in the above-mentioned collector field. At the 1st process of the above In the above-mentioned base region, the 1st conductivity-type impurity can be introduced, the emitter region of the above-mentioned bipolar transistor can be formed, and nitrogen can be introduced into a field including a part of above-mentioned emitter region [at least] at the 2nd process of the above.

[0108] By this approach, a bipolar transistor with a high current amplification factor can be formed.

[0109] It sets to claims 34, 35, 36, and 37 or 38 as indicated by claim 47. The process which prepares a bipolar transistor formation field, introduces the 1st conductivity-type impurity into the above-mentioned bipolar transistor formation field, and forms the collector field of a bipolar transistor in the above-mentioned semi-conductor substrate, It has further the process which introduces the 1st conductivity-type impurity in the above-mentioned collector field, and forms the emitter region of the above-mentioned bipolar transistor after the 1st process of the above. At the 2nd process of the above The 2nd conductivity-type impurity is introduced into the field which encloses the inside of the above-mentioned collector field, and the above-mentioned emitter region, the base region of a bipolar transistor can be formed and nitrogen can be introduced into a field including a part of above-mentioned base region [at least] at the 2nd process of the above.

[0110] By this approach, a bipolar transistor with high cut-off frequency can be formed.

[0111]

[Embodiment of the Invention]

(1st operation gestalt) Drawing 1 (a) - (d) is the sectional view showing the process of the 1st nMOS mold field-effect transistor.

[0112] First, at the process shown in

drawing 1 (a), after forming isolation 4 in a part of silicon substrate 1, forming the oxide film whose thickness is 7nm by thermal oxidation etc. on the silicon substrate 1 in the active region surrounded by isolation 4 and depositing further the polish recon film whose thickness is 150nm on it, patterning of an oxide film and the polish recon film is carried out according to photolithography and a dry etching process, and gate oxide 2 and the gate electrode 3 are formed. In addition, in order to secure the conductivity of the gate electrode 3, n mold impurity is doped by the polish recon film by the ion implantation after the time of the deposition by the CVD method, or deposition. This is the same also in each operation gestalt mentioned later.

[0113] Next, at the process shown in drawing 1 (b), nitrogen ion (N+) is poured in energy 10keV and dose 1x1015cm-2 with 4 step ion-implantation from the direction which inclined aslant [25 degree] to the direction vertical to a semi-conductor substrate side in the cross section parallel to the direction of a channel of a transistor. In that case, with 4 step ion-implantation, the direction of grouting of impurity ion is fixed and impurity ion is poured in in four locations which carried out the sequential revolution of every 90 degrees of the silicon substrates 1 in the level surface. Then, nitrogen ion is diffused by heat treatment and nitrogen diffusion layer 6a is formed in the both ends of gate oxide 2 for acid nitrated case 5a in a silicon substrate 1, respectively. At this process, it is the impregnation energy of nitrogen ion. Whenever [1x1013-5x1015cm-2 and angle-of-inclination / of a direction of grouting] has [5 - 20keV and a dose] 7 degrees - desirable 45 degrees.

[0114] In addition, although impurity ion is driven into the ends of gate oxide 2 with this operation gestalt since nitrogen ion is poured in with 4 step ion-implantation, impurity ion may be poured in from one direction which only inclined to the drain field side. Moreover, the direction which drives in impurity ion does not necessarily need to be in agreement in the direction of a channel of a transistor (that is, direction parallel to the space of drawing 1). That is, if the include angle between the line projected on the field (space of drawing 1) where the direction of ion implantation intersects perpendicularly in the gate width direction, and the normal of a substrate side is 10 degrees or more, the effectiveness of this invention can be demonstrated. The above-mentioned thing is the same also about each next operation gestalt.

[0115] Next, at the process shown in drawing 1 (c), mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured in by energy 10keV and dose 1x1015cm-2,

and n mold low concentration source drain field 7 is formed in the field near the front face in a silicon substrate 1. In addition, since nitrogen diffusion layer 6a is formed in the silicon substrate 1, a channeling is not produced even if it pours in impurity ion perpendicularly.

[0116] Next, at the process shown in drawing 1 (d), after depositing thicker silicon oxide on a substrate, etchback is performed, after forming a sidewall 8 on the both-sides side of the gate electrode 3, further mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured in by energy 30keV and dose 5x1015cm-2, and n mold high concentration source drain field 9 is formed in the both sides of a sidewall 8.

[0117] Unlike the structure of a transistor where the above-mentioned conventional acid nitrated case was prepared in the nMOS mold field-effect transistor formed of the production process of this operation gestalt, acid nitrated case 5a is formed only in the both ends of gate oxide 2. Generally, the cause of main of hot carrier degradation is for a hot carrier to be captured by the gate oxide by the side of a drain. Therefore, like this operation gestalt, if acid nitrated case 5a is formed in the edge by the side of a drain (this operation gestalt both ends) even if there is little gate oxide 2, hot carrier degradation can be prevented.

[0118] Since what is necessary is to inject nitrogen ion only into the edge of gate oxide 2 by the ion implantation from a large inclination in this way, even if it is about [1x1015cm -] two low dose and pours in nitrogen ion with low impregnation energy called 10keV(s) on the other hand, acid nitrated case 5a can be formed. Since the dose of nitrogen ion needed to be made deep when an acid nitrated case was formed the whole region in gate oxide like the above-mentioned conventional approach, depletion-ization of a gate electrode had been caused. To it, by the approach of this operation gestalt, since doses may be few, depletion-ization of the gate electrode 3 is not caused.

[0119] Moreover, since the depth of nitrogen diffusion layer 6a formed in a silicon substrate 1 at the process shown in drawing 1 (b) is also shallow, the fields where crystallinity was confused are few parts. Furthermore, since the concentration of the nitrogen ion in nitrogen diffusion layer 6a is also low, the degree of the turbulence of crystallinity in a silicon substrate 1 can also be minimized. Therefore, degradation of the engine performance of a transistor can be controlled and improvement in the dependability of a transistor can be aimed at.

[0120] In addition, with this operation gestalt, although acid nitrated case 5a was formed in the both ends of gate oxide 2, even if there is little gate oxide 2, acid

nitrated case 5a should just be formed in the edge by the side of a drain. This is the same also in each below-mentioned operation gestalt.

[0121] (2nd operation gestalt) Drawing 2 (a) - (d) is the sectional view showing the process of the nMOS mold field-effect transistor concerning the 2nd operation gestalt.

[0122] First, isolation 4 is formed in a part of silicon substrate 1 at the process shown in drawing 2 (a). The oxide film whose thickness is 7nm is formed by thermal oxidation etc. on the silicon substrate 1 in the active region surrounded by isolation 4. After depositing on it the polish recon film whose thickness is 150nm, and the oxide film whose thickness is 150nm furthermore, patterning of two oxide films and the polish recon film is carried out according to photolithography and a dry etching process. Gate oxide 2, the gate electrode 3, and the gate top oxide film 10 are formed.

[0123] Next, at the process shown in drawing 2 (b), nitrogen ion (N+) is poured in with 4 step ion-implantation energy 10keV and dose 1x1015cm-2 from the direction to which 25 degrees inclined to the direction of a normal of a substrate to the direction vertical to the front face of a silicon substrate 1. In that case, with 4 step ion-implantation, the direction of grouting of impurity ion is fixed and impurity ion is poured in in four locations which carried out the sequential revolution of every 90 degrees of the silicon substrates 1 in the level surface. Then, nitrogen ion is diffused by heat treatment and nitrogen diffusion layer 6a is formed in the both ends of gate oxide 2 for acid nitrated case 5a in a silicon substrate 1, respectively. At this process, the impregnation energy of nitrogen ion is 5 - 30keV, and 7 degrees - 45 degrees of a dose are [whenever / 1x1013-5x1016cm-2 and angle-of-inclination / of a direction of grouting] desirable.

[0124] Next, at the process shown in drawing 2 (c), mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured in by energy 10keV and dose 1x1014cm-2, and n mold low concentration source drain field 7 is formed in the field near the front face in a silicon substrate 1.

[0125] Next, at the process shown in drawing 2 (d), after depositing thicker silicon oxide on a substrate, etchback is performed, after forming a sidewall 8 on the both-sides side of the gate electrode 3, further mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured in by energy 30keV and dose 5x1015cm-2, and n mold high concentration source drain field 9 is formed in the both sides of a sidewall 8.

[0126] With this operation gestalt, since the gate top oxide film 10 is formed on the gate electrode 3 in addition to the

effectiveness of the 1st above-mentioned operation gestalt, in the process shown in drawing 2 (b), the nitrogen volume poured in into the gate electrode 3 decreases substantially. Therefore, property degradation of the transistor by depletion-izing of the gate electrode 3 can be controlled more certainly. Moreover, since depletion-ization of the gate electrode 3 is not caused even if it increases the impregnation energy and the injection rate of nitrogen ion, the selection width of face of conditions can be expanded.

[0127] (3rd operation gestalt) Drawing 3 (a) - (d) is the sectional view showing the process of the CMOS device concerning the 3rd operation gestalt.

[0128] First, at the process shown in drawing 3 (a), the form of the isolation 4 which divides the pMOSFET formation field Rpfet which is the nMOSFET formation field Rnfet and the 2nd active region which are the 1st active region on a silicon substrate 1 is carried out. And after forming the oxide film whose thickness is 7nm by thermal oxidation etc. on the silicon substrate 1 in each fields Rnfet and Rpfet surrounded by isolation 4 and depositing further the polish recon film whose thickness is 150nm on it, patterning of an oxide film and the polish recon film is carried out according to photolithography and a dry etching process, and gate oxide 2 and the gate electrode 3 are formed in each fields Rnfet and Rpfet, respectively. In addition, in order to secure the conductivity of the gate electrode 3, n mold impurity and p mold impurity are doped by the polish recon film on each fields Rnfet and Rpfet, respectively by the ion implantation after the time of the deposition by the CVD method, or deposition. the 4- which this mentions later -- also in the 6th operation gestalt, it is the same.

[0129] Next, at the process shown in drawing 3 (b), form the wrap photoresist film Fr1 for the pMOSFET formation field Rpfet, and this photoresist film Fr1 is used as a mask. With 4 step ion-implantation from the direction which inclined aslant [25 degree] to the direction vertical to the front face of a silicon substrate 1 After pouring in nitrogen ion (N+) by energy 10keV and dose 1x1015cm-2, Nitrogen ion is diffused by heat treatment and nitrogen diffusion layer 6a is formed in the both ends of the gate oxide 2 of the nMOSFET formation field Rnfet for acid nitrated case 5a in a silicon substrate 1, respectively. And it progresses to the following process, without forming acid nitrated case 5a and nitrogen diffusion layer 6a in the pMOSFET formation field Rpfet.

[0130] Next, at the process shown in drawing 3 (c), the photoresist film is formed according to an individual in the nMOSFET formation field Rnfet and the pMOSFET formation field Rpfet (not shown), and the low concentration source

drain fields 7 and 12 are formed in each fields Rnfet and Rpfet, respectively. That is, mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured into the nMOSFET formation field Rnfet by energy 10keV and dose 1x1014cm-2, and n mold low concentration source drain field 7 is formed in it. Mostly, with the ion-implantation from a perpendicular direction, boron fluoride ion (BF2+) is poured into the pMOSFET formation field Rpfet by energy 10keV and dose 1x1014cm-2, and p mold low concentration source drain field 12 is formed in it.

[0131] Next, at the process shown in drawing 3 (d), after depositing thicker silicon oxide on a substrate, etchback is performed, after forming a sidewall 8 on the both-sides side of the gate electrode 3, the photoresist film is formed according to an individual in the nMOSFET formation field Rnfet and the pMOSFET formation field Rpfet (not shown), and the high concentration source drain fields 9 and 13 are formed in each fields Rnfet and Rpfet. That is, in the nMOSFET formation field Rnfet, mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured in by energy 30keV and dose 5x1015cm-2, and n mold high concentration source drain field 9 is formed in the both sides of a sidewall 8. In the pMOSFET formation field Rpfet, mostly, with the ion-implantation from a perpendicular direction, boron fluoride ion (BF2+) is poured in by energy 30keV and dose 5x1015cm-2, and p mold high concentration source drain field 13 is formed in the both sides of a sidewall 8.

[0132] With this operation gestalt, since nitrogen is eventually injected only into a nMOS mold field-effect transistor and acid nitrated case 5a and nitrogen diffusion layer 6a are formed, in addition to the effectiveness of the operation gestalt of the above 3rd, degradation of the mutual conductance in a pMOS mold field-effect transistor can be controlled.

[0133] (4th operation gestalt) Drawing 4 (a) - (d) is the sectional view showing the production process of the CMOS device concerning the 4th operation gestalt.

[0134] With this operation gestalt, if the point that the gate top oxide film 10 is formed on the gate electrode 3 is removed at the process shown in drawing 4 (a), the same processing as the process shown in drawing 3 (a) - (d) in the operation gestalt of the above 3rd will be performed.

[0135] Therefore, with this operation gestalt, since the nitrogen volume poured in into the gate electrode 3 with the gate top oxide film 10 is reduced substantially in addition to the same effectiveness as the operation gestalt of the above 3rd, degradation of the engine performance of the transistor resulting from depletion-ization of the gate electrode 3 can be prevented more certainly.

[0136] (5th operation gestalt) Drawing 5 (a) - (e) is the sectional view showing the production process of the CMOS device concerning the 5th operation gestalt.

[0137] First, isolation 4 is formed in a part of silicon substrate 1 at the process shown in drawing 5 (a). The oxide film whose thickness is 7nm is formed by thermal oxidation etc. on the silicon substrate 1 in the active region surrounded by isolation 4. After thickness furthermore deposits on it the polish recon film which is 150nm, patterning of an oxide film and the polish recon film is carried out according to photolithography and a dry etching process. Gate oxide 2 and the gate electrode 3 are formed in the nMOSFET formation field Rnfet and the pMOSFET formation field Epfet, respectively.

[0138] Next, at the process shown in drawing 5 (b), form the wrap photoresist film Fr1 for the pMOSFET formation field RPfet, and this photoresist film Fr1 is used as a mask. With 4 step ion-implantation from the direction which inclined aslant [25 degree] to the direction vertical to the front face of a silicon substrate 1 After pouring in nitrogen ion (N+) by energy 10keV and dose 1x1015cm-2, Nitrogen ion is diffused by heat treatment and nitrogen diffusion layer 6a is formed in the both ends of the gate oxide 2 of the nMOSFET formation field Rnfet for acid nitrated case 5a in a silicon substrate 1, respectively.

[0139] Next, at the process shown in drawing 5 (c), the wrap photoresist film Fr2 is formed for the nMOSFET formation field Rnfet, by using this photoresist film Fr2 as a mask, mostly, with the ion-implantation from a perpendicular direction, after pouring in nitrogen ion (N+) by energy 10keV and dose 1x1015cm-2, nitrogen ion is diffused by heat treatment and the nitrogen diffusion layer 6 is formed in the silicon substrate 1 of the pMOSFET formation field Rpfet. In addition, the weak acid nitrated case 5 is formed in gate oxide 2.

[0140] Next, at the process shown in drawing 5 (d), the photoresist film is formed according to an individual in the nMOSFET formation field Rnfet and the pMOSFET formation field Rpfet (not shown), and the low concentration source drain fields 7 and 12 are formed in each fields Rnfet and Rpfet, respectively. That is, mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured into the nMOSFET formation field Rnfet by energy 10keV and dose 1x1014cm-2, and n mold low concentration source drain field 7 is formed in it. Mostly, with the ion-implantation from a perpendicular direction, boron fluoride ion (BF2+) is poured into the pMOSFET formation field Rpfet by energy 10keV and dose 1x1014cm-2, and p mold low concentration source drain field 12 is formed in it.

[0141] Next, at the process shown in drawing 5 (e), after depositing thicker silicon oxide on a substrate, etchback is performed, after forming a sidewall 8 on the both-sides side of the gate electrode 3, the photoresist film is formed according to an individual in the nMOSFET formation field Rnfet and the pMOSFET formation field Rpfet (not shown), and the high concentration source drain fields 9 and 13 are formed in each fields Rnfet and Rpfet. That is, in the nMOSFET formation field Rnfet, mostly, with the ion-implantation from a perpendicular direction, arsenic ion (As+) is poured in by energy 30keV and dose 5x1015cm-2, and n mold high concentration source drain field 9 is formed in the both sides of a sidewall 8. In the pMOSFET formation field Rpfet, mostly, with the ion-implantation from a perpendicular direction, boron fluoride ion (BF2+) is poured in by energy 30keV and dose 5x1015cm-2, and p mold high concentration source drain field 13 is formed in the both sides of a sidewall 8.

[0142] Although the CMOS device formed of the production process of this operation gestalt has the almost same structure as the CMOS mold device formed by the production process of the operation gestalt of the above 3rd, unlike the above-mentioned 3rd operation gestalt, the nitrogen diffusion layer 6 is formed in the silicon substrate 1 of a pMOS mold field-effect transistor. Therefore, in addition to the effectiveness of the 3rd above operation gestalt, and the same effectiveness, it is effective in preventing the channeling at the time of an ion implantation also in the pMOSFET formation field Rpfet, and it is stabilized and a source drain field can be formed. Moreover, in a pMOS mold field-effect transistor, mostly, since an acid nitrated case is slightly formed in the gate electrode 3 of gate oxide 2 of impregnation of the nitrogen ion from a perpendicular direction, there is also an advantage which can be controlled as much as possible about the boron in the gate electrode 3 running in a silicon substrate side.

[0143] (6th operation gestalt) Drawing 6 (a) - (e) is the sectional view showing the production process of the CMOS device concerning the 6th operation gestalt.

[0144] According to the production process of this operation gestalt, the almost same process as the operation gestalt of the above 5th is performed, and only the point which forms the gate top oxide film 10 on the gate electrode 3 differs from the 5th operation gestalt in the condition which shows in drawing 6 (a).

[0145] In the CMOS device formed of the production process of this operation gestalt, since the gate top oxide film 10 is formed on the gate electrode, in addition to the same effectiveness as the operation gestalt of the above 5th, the nitrogen

volume poured in into the gate electrode 3 can be reduced substantially. Therefore, degradation of the property of the transistor resulting from depletion-ization of the gate electrode 3 can be prevented more certainly.

[0146] (7th operation gestalt) Drawing 7 is the sectional view showing the production process of the semiconductor device in this operation gestalt, and it decides to explain the process for improving distribution of the high impurity concentration in p mold diffusion layer with this operation gestalt, referring to drawing 7 (a)-(c).

[0147] First, at the process shown in drawing 7 (a), boron ion (B+) is injected into n mold silicon substrate 21 by acceleration energy 10keV and dose 2x1015cm-2. At this time, he is BF2 instead of boron ion. Ion may be poured in by acceleration energy 30keV and dose 2x1015cm-2. Boron or BF2 By pouring in ion, p mold diffusion layer 22 to which activation is performed behind is formed.

[0148] Next, at the process shown in drawing 7 (b), a substrate is installed in usual rapid heating heat treatment (Rapid Thermal Annealing) equipment, and heat treatment is performed for 900 degrees C and 10 seconds in the ammonia gas ambient atmosphere where the ammonia gas for 5l./was passed. Thereby, nitrogen is introduced in a silicon substrate 21 and boron and the nitrogen mixture layer 23 (nitrogen diffusion layer) are formed in a field until it reaches the predetermined depth from the front face of a silicon substrate 1.

[0149] Furthermore, using rapid heating heat treatment (Rapid Thermal Annealing) equipment, by performing heat treatment for the activation for 10 seconds at 1000 degrees C, it is spread as if the boron within p mold diffusion layer 22 (or BF2) is activated, and the range of p mold diffusion layer 22 usually becomes settled at the process shown in drawing 7 (c). In addition, nitrogen is also diffused with boron (or BF2).

[0150] Drawing 8 shows the concentration profile in the boron and the depth direction of BF2 (concentration distribution curves L1 and L2 of a continuous line), and nitrogen (concentration distribution curve Ln of a broken line) of [within p mold diffusion layer 22 formed of this operation gestalt]. In addition, the boron at the time of performing heat treatment for activation, without performing rapid heating heat treatment in an ammonia gas ambient atmosphere for a comparison and BF2 The concentration distribution curves L3 and L4 (dotted line) are shown. However, p mold diffusion layer formed by the manufacture approach of this operation gestalt in the following explanation, That is, what has the source drain field which performed rapid heating heat treatment in an ammonia gas ambient atmosphere after pouring in boron is made into

Sample a. He is BF2 at 30keV(s). p mold diffusion layer which performed rapid heating heat treatment in the ammonia gas ambient atmosphere after pouring in ion is made into Sample b. After pouring in boron ion by 10keV(s), p mold diffusion layer which omits rapid heating heat treatment in an ammonia gas ambient atmosphere is made into Sample c, and he is BF2 at 30keV. After pouring in ion, p mold diffusion layer which omits rapid heating heat treatment in an ammonia gas ambient atmosphere is called sample d. However, BF2 Impregnation energy differs for compensating a difference of the impregnation depth resulting from a mass difference by the case where the case where ion is poured in, and boron ion pour in.

[0151] As shown in this drawing, since the field in about 0.1-micrometer Fukashi serves as boron and the nitrogen mixture layer 23 among the original impurity diffused layers 22, the concentration profile curve L1 of the sample a which introduced boron and nitrogen and carried out rapid heating heat treatment in the ammonia gas ambient atmosphere has the description that the boron concentration within this boron and nitrogen mixture layer 23 is high. The reduction rate of the concentration become small near [a certain / point Pch1], and the concentration of the boron in Sample a turn into concentration near the sample c which concentration decrease comparatively gently and have not introduce nitrogen after that, although concentration decrease rapidly after pass the peak location Peb compared with the sample c (curve L3) which have not introduce nitrogen (field L1a in drawing) (field L1b in drawing). In other words, the point Pch1 in drawing is equivalent to the point of inflection of the concentration when making concentration into the function of the depth. Concentration distribution of the boron in Sample a shows such a gestalt for the inclination for diffusion of boron to be controlled with the nitrogen in boron and the nitrogen mixture layer 23, consequently for the boron after activation to be unevenly distributed in the field (for it to be the upper part from the location whose depth is about 0.1 micrometers) where the concentration of nitrogen is high in the case of heat treatment for activation arising.

[0152] In addition, conventionally, although installation of the nitrogen into a semi-conductor substrate is proposed, it is performed by impregnation of nitrogen ion in that case. And using general common sense, it was thought that the nitrogen which has meaning practical in a semi-conductor substrate depending on heat treatment in nitrogen-gas-atmosphere mind, such as ammonia gas, could not be introduced. However, it is conditions like this operation gestalt, that is, by performing

comparatively hot rapid heating processing in an ammonia gas ambient atmosphere showed that a comparatively high-concentration nitrogen diffusion layer could be formed in a silicon substrate.

[0153] And unlike the case where nitrogen ion is poured in into a silicon substrate depending on the introductory approach of the nitrogen by heat treatment like this operation gestalt, a defect is not produced in a silicon substrate. Therefore, it turns out that the defect was produced in the case of installation of nitrogen, and diffusion of an impurity was not controlled according to this defect. Moreover, BF2 The impurity atom concentration profile curve L4 of the sample d which performed activation, without introducing and introducing nitrogen shows the reduction property gently-sloping on the whole for peak value after owner Perilla frutescens (L.) Britton var. crispa (Thunb.) Decne. very near the front face, and its peak value is also small. This is BF2 by existence of fluorine ion. It is considered because diffusion is controlled on the whole. Therefore, BF2 The high-impurity-concentration profile which had the description like this operation gestalt depending on installation cannot be obtained.

[0154] On the other hand, he is BF2. And the concentration distribution curve L2 of the sample b which introduced nitrogen and carried out rapid heating heat treatment in the ammonia gas ambient atmosphere has point of inflection Pch2 in the 0.07 neighborhoods where the depth is smaller than 0.1 micrometers. Therefore, a high concentration field can be centralized on the in this case still smaller range.

[0155] Although it is some specific conditions and the concentration profile at the time of performing rapid heating heat treatment in installation of nitrogen and an ammonia gas ambient atmosphere was shown in drawing 8 , it is possible by adjusting temperature, time amount, etc. of rapid heating heat treatment in an ammonia ambient atmosphere, or changing operation sequence of the impregnation process of boron ion, and the rapid heating heat treatment process in an ammonia gas ambient atmosphere to control the concentration profile of boron.

[0156] Moreover, it is desirable to perform rapid heating processing in an ammonia gas ambient atmosphere on 900 degrees C or more and the conditions for 10 or less seconds. It is because ammonia gas is pyrolyzed above 800 degrees C and it generally activates more above 900 degrees C. However, it is [that it should already control diffusion of these impurities in case p mold impurity **** introduces nitrogen into the source drain field to which n mold impurity was introduced by rapid heating processing]

desirable to carry out on conditions 1050 degrees C or less in 1000 degrees C or less and a nMOS transistor with a pMOS transistor. Although an ammonia quantity of gas flow is generally 1 - 10slm extent, it is not limited to this. It is checked by performing pulse-heating especially, so that the heating processing time may be cooled in an instant, if it is very short, for example, target temperature is reached that the concentration distribution near [which is shown in the concentration distribution curve L1 of drawing 8] the front face of a concentration profile becomes still steeper. That is, peak value Peb becomes still higher, and it is point of inflection Pch1. It moves to a left.

[0157] Furthermore, it is also possible to communalize the rapid heating heat treatment process in an ammonia gas ambient atmosphere and the heat treatment process for impurity activation, or it is also possible to consider two processes as multistage processing and they to carry out consecutive processing.

[0158] In addition, they are boron or BF2 in a semi-conductor substrate. Even if the conditions at the time of pouring in change somewhat, the same effectiveness as this operation gestalt can be demonstrated by choosing suitably the rapid heating heat treatment conditions in a subsequent ammonia gas ambient atmosphere.

[0159] Moreover, as an impurity for carrier generation introduced in a semi-conductor substrate, it is applicable not only to boron but Lynn, arsenic, in JUUMU, antimony, etc. Moreover, there is not only the impurity for carrier generation but effectiveness which controls diffusion of the impurity which does not generate carriers, such as a fluorine, by introducing nitrogen. That is, the effectiveness of making point of inflection produce is in the concentration profile curve.

[0160] In addition, even if it performs rapid heating heat treatment in the gas ambient atmosphere which added inert gas, such as nitrogen gas and argon gas, in ammonia gas, the same effectiveness as this operation gestalt is expectable. Moreover, inside of the mixed-gas ambient atmosphere of nitrogen gas and other gas, such as hydrogen gas, and NF3 Even if it performs rapid heating heat treatment in a gas ambient atmosphere, the same effectiveness as this operation gestalt is acquired.

[0161] Furthermore, the semiconductor regions in this invention may be polycrystal semiconductor regions, such as for example, not only the single crystal semiconductor region in a semi-conductor substrate but polish recon, and amorphous semiconductor fields, such as an amorphous silicon. In order to raise conductivity also in a polycrystal semiconductor region or an amorphous semiconductor field, the same

high-impurity-concentration profile as this operation gestalt can be made to produce by introducing nitrogen into the field to which impurities for carrier generation, such as boron, phosphorus, and arsenic, may be introduced, and the impurity concerned was introduced also in this case.

[0162] (8th operation gestalt) Next, the 8th operation gestalt which is the example which used the amelioration technique of the impurity atom concentration profile in the 7th above-mentioned operation gestalt for the improvement of the property of a pMOS device is explained. Drawing 9 is flow drawing showing the procedure of the production process of this operation gestalt, and drawing 10 is the sectional view showing the production process of the pMOS device concerning this operation gestalt.

[0163] first -- the process shown in drawing 10 (a) -- the inside of a semi-conductor substrate -- n -- a well 31 -- forming -- this n -- after forming the oxide film whose thickness is about 4nm on a well 31 and forming further the polish recon film whose thickness is about 200nm on gate oxide 32, patterning of an oxide film and the polish recon film is carried out according to a lithography process and a reactive-ion-etching (RIE) process, and gate oxide 32 and the gate electrode 33 are formed. Then, using the gate electrode 33 as a mask, acceleration energy is about 10 keV(s) and a dose is BF2 at the conditions of abbreviation 1x1014cm-2. Ion is poured in and the extension field 34 (p mold diffusion layer) of a source drain is formed. Furthermore, acceleration energy forms the pocket field 35 (n mold diffusion layer) for pouring in arsenic ion on the conditions abbreviation 6x1012cm-2 and whose impregnation include angles about 160 keV(s) and a dose are about 20 degrees, and raising punch-through pressure-proofing by using the gate electrode 33 as a mask.

[0164] Then, at the process shown in drawing 10 (b), after depositing an oxide film with a thickness of 120nm by LPCVD by TEOS gas, by dry etching, etchback of this oxide film is carried out, on the both-sides side of the gate electrode 33, some oxide films are made to remain and a sidewall 36 is formed. Furthermore, acceleration energy performs about 10 keV(s) on condition that abbreviation 2x1015cm-2, a dose pours in boron ion, and the source drain field 37 (p mold diffusion layer) is formed. At this time, boron is introduced also into the gate and it becomes the electrode of p mold transistor.

[0165] Then, at the process shown in drawing 10 (c), a substrate is installed in usual rapid heating heat treatment (RapidThermal Annealing) equipment, and it heat-treats in the ammonia ambient atmosphere which poured 5l. the ammonia for /, and on condition that for

about 900 degrees C and about 10 seconds. Thereby, nitrogen is introduced in a semi-conductor substrate and boron and the nitrogen mixture layer 38 (nitrogen diffusion layer) are formed in the field near a front face among the source drain fields 37. Furthermore, the range of the extension field 34 of p mold, the source drain field 37 of p mold, and the pocket field 35 of n mold becomes settled by adding about 1000 degrees C and heat treatment for about 10 seconds as heat treatment for activating an impurity with usual rapid heating heat treatment (Rapid Thermal Annealing) equipment. At this time, nitrogen is similarly spread by high concentration in about 0.1-micrometer Fukashi in the source drain field 37 in p mold diffusion layer 22 of the operation gestalt of the above 1st. Therefore, the concentration profile of the boron in the source drain field 37 is mostly in agreement with the profile shown in drawing 8 . That is, it has the concentration profile which the field where high-concentration boron exists concentrated near the front face. Moreover, since diffusion of an impurity is controlled with nitrogen in the extension field 34, comparatively high-concentration boron exists in the field near a front face in in the extension field 34, and it has the concentration profile which shows a steep concentration gradient (reduction in concentration) directly under the.

[0166] In addition, although the impurity for forming the extension field 34 and the pocket field 35 in the source drain field 37 is also introduced with this operation gestalt, since it is a minute amount compared with the high impurity concentration for source drain formation, existence of those impurities can be mostly disregarded in the source drain field 37. However, the configuration of the source drain field 37 can be affected so that it may mention later.

[0167] Then, at the process shown in drawing 10 (d), 30nm of refractory metals like titanium is deposited by the sputtering method, and 700 degrees C and heat treatment for 1 minute are added. Since the field near [which consists of a source drain field 37 which consists of silicon, or polish recon by this heat treatment] the front face of gate electrode 33 grade reacts with titanium, the titanium silicide film 39 is formed near the front face of source drain field 37a or the gate electrode 33. Then, the unreacted titanium film which was not silicide-ized is removed by wet etching. Furthermore, after that, an interlayer insulation film 40, the embedding plug 41 to a contact hole, wiring (not shown), etc. are formed on a substrate, and the p mold MOSFET of a surface channel mold is manufactured.

[0168] By making it the above manufacture approaches, since the high concentration field in the source drain

field 37 and the comparatively high-concentration field in extension field 34a are concentrated near a front face by the diffusion depressant action of the impurity by nitrogen, punch-through pressure-proofing of a transistor improves and the control function of a short channel effect also improves by it. This point is explained in detail later.

[0169] Next, the measurement result about the property of the transistor which followed this operation gestalt is explained. However, the p mold MOSFET formed by the manufacture approach of the gestalt this operation in the following explanation That is, what has the source drain field which performed rapid heating heat treatment in an ammonia gas ambient atmosphere after pouring in boron is made into Sample A. He is BF2 at 30keV(s). The p mold MOSFET which performed rapid heating heat treatment in the ammonia gas ambient atmosphere after pouring in ion is made into Sample B. The p mold MOSFET which omits rapid heating heat treatment in the ammonia gas ambient atmosphere after pouring in boron ion by 10keV(s) is made into Sample C. He is BF2 at 30keV(s). After pouring in ion, the p mold MOSFET which omits rapid heating heat treatment in the ammonia gas ambient atmosphere is called sample D. However, BF2 Impregnation energy differs for compensating a difference of the impregnation depth resulting from a mass difference by the case where the case where ion is poured in, and boron ion pour in.

[0170] Drawing 11 is property drawing showing the gate length dependency of Samples A and C and the threshold electrical potential difference about D. However, it is shown that a short-channel-effect control function is so large that extent from which a threshold electrical potential difference changes with gate length is small. Drawing 12 is data in which the result of having measured both transistor characteristics (I-V property) is shown after forming Samples A and D so that gate length and a threshold electrical potential difference may become almost the same. Drawing 13 is data in which change of the contact resistance of the interface concerned to the area of the interface between silicide film-source drain fields when forming the silicide film on a source drain field further is shown about Samples A, B, C, and D.

[0171] When it compares about what poured in boron ion by 10keV(s) so that drawing 11 may show, the control function of a short channel effect is large than the sample C which did not perform rapid-heating heat treatment in an ammonia gas ambient atmosphere, and the sample A of this operation gestalt which performed rapid-heating heat treatment in an ammonia gas ambient atmosphere is BF2. After pouring in ion

by 30keV(s), it has a short-channel-effect control function equivalent to the sample D which omits rapid-heating heat treatment in the ammonia ambient atmosphere. On the other hand, when the transistor characteristics of Samples A and D are compared so that drawing 12 may show, the sample A of this operation gestalt of a saturation drain current which performed rapid heating heat treatment in the ammonia gas ambient atmosphere by boron 10keV impregnation is larger 15%. This is considered to originate in that the direction of the sample A of this operation gestalt has low resistance of the interface between silicide film-source drain fields shown in drawing 13 , and resistance of the source drain field of Sample A being low since high impurity concentration [in / as shown in drawing 8 / by boron 10keV impregnation / in the skirt of the profile of a source drain field / broadcloth, i.e., the field of the method of the back of a source drain field,] is high. That is, the MOS device of this operation gestalt is BF2. Compared with the MOS device which performs only impregnation of ion and omits rapid heating heat treatment in an ammonia gas ambient atmosphere, although the short-channel-effect control function is equivalent, it can realize a bigger saturation drain current.

[0172] In addition, drawing 14 shows the data which compare the gate width dependency of the n-ch gate resistance about the n mold MOSFET which performed rapid heating heat treatment in an ammonia gas ambient atmosphere after impregnation of arsenic ion, and the n mold MOSFET which omits rapid heating heat treatment in an ammonia gas ambient atmosphere. Moreover, drawing 15 is data in which the silicide width-of-face dependency of the sheet resistance in the source drain field of the above-mentioned samples A, B, C, and D of the p mold MOSFET is shown. As shown in drawing 14 , nonconformity which checks the object of the silicide technique of attaining low resistance-ization by silicide-ization is not produced by introducing nitrogen like this operation gestalt. Although it is generally pointed out that silicide-ized processing is checked by installation of nitrogen, since the concentration of nitrogen is a minute amount very much, by the approach of this operation gestalt, it turns out that this nonconformity has not arisen. Moreover, he is BF2 as shown in drawing 15 . It turns out that the nonconformity of buildup of the sheet resistance by impregnation of ion is eased by installation of nitrogen. That is, BF2 In impregnation of ion, since the peak value of high impurity concentration is in near very much, it is known [for which formation of the uniform silicide film is checked] about the front face, but since the peak value of high impurity concentration exists for a while rather

than a front face a downward location, i.e., directly under [which are silicide-ized] a field, in impregnation of boron ion, formation of the uniform silicide film is not checked. And sheet resistance is substantially improvable with the MOS device of this operation gestalt by making high high impurity concentration of the field directly under the silicide film which achieves the function most important for reduction of sheet resistance.

[0173] In addition, it turns out that the higher efficacy which is junction leak that it can also decrease is obtained.

[0174] Next, the structural feature and advantage which are produced by introducing nitrogen into the source drain field of MOSFET are explained.

[0175] Drawing 16 is the sectional view showing the structure the general source drain field of MOSFET, and near a channel field. However, only the drain field is shown in this drawing, and since the source field generally has a drain field and symmetrical structure, the graphic display is omitted. Moreover, drawing 17 is drawing which took out the impurity atom concentration profile curves L1 and L2 to the depth direction of a substrate from the data in above-mentioned drawing 8 about the source drain field which introduced the boron and nitrogen of this operation gestalt, and the source drain field only by the conventional boron impregnation. The conventional source drain field SDb formed of installation of only boron ion as shown in drawing 16 It has a configuration as generally shown with a broken line. Generally, diffusion (the both sides of diffusion by the ion implantation and diffusion by heating are included) of an impurity progresses in each direction at a fixed rate from the source of diffusion at homogeneity. And it is because the front face of a source drain field is equivalent to the source of diffusion in this case, so diffusion will advance from straight-line-like the source of diffusion in the cross section shown in drawing 1616 . On the other hand, the source drain field SDbn of an operation gestalt shows the configuration shown as the continuous line in drawing. It is thought that it is based on the following reasons that such a difference arises.

[0176] A source drain field can be divided roughly into the field Rch contiguous to a channel field, the field Rpa used as the direction which produces a punch through, and the field Rsb of the pars basilaris ossis occipitalis which adjoins a substrate field. On the other hand, in the semi-conductor substrate, n mold impurities for threshold control (arsenic, phosphorus, etc.) and n mold impurity for punch-through prevention are doped, and the high concentration field of this n mold impurity exists in a certain depth range which went into the method of the back from the front face of a semi-conductor substrate (refer to drawing 17). The

source drain field SDbn which starts this operation gestalt from the above thing is the conventional source drain field SDb. It receives and the following geometrical descriptions are shown. First, it sets to the field Rch near a substrate front face, and the high impurity concentration in the source drain field SDbn of this operation gestalt is the conventional source drain field SDb. Since it is deeper than inner concentration, in the field Rch near a front face, the source drain field SDbn of this operation gestalt is the conventional source drain field SDb. It has pushed out to the channel field side. This is because it can pour in with bigger energy than the conditions when not introducing nitrogen at the time of the ion implantation of the impurity for source drain formation by the ability restricting a high concentration field to the narrow field near a front face. And in the field Rpa deeper than a channel field, since the high impurity concentration in the source drain field of this operation gestalt falls rapidly after it passes over a peak, it receives strongly the effectiveness of reducing the carrier generation by n mold impurity. Therefore, in Field Rpa, it retreats in the direction which keeps away from a channel field from the source drain field SDbf of the conventional MOSFET. Furthermore, the field Rsb of the pars basilaris ossis occipitalis of a source drain field is the source drain field SDb when not introducing nitrogen by the ability of ion-implantation energy to be enlarged like ****. It becomes deep. That is, the concentration distribution in the method of the substrate back of the source drain field SDbn of this operation gestalt shows broadcloth distribution compared with the concentration distribution when not introducing nitrogen, and the source drain field SDbn becomes deep.

[0177] And MOSFET of this operation gestalt has the advantage of the following letters of actuation by the above structural feature. First, parasitism resistance becomes small when the field Rch near a substrate front face has pushed out to the channel field side. And the resistance over a punch through becomes large and the control function of a short channel effect becomes large because the field [directly under] Rpa of it is retreating. Furthermore, since the dip in Field Rpa is loose, parasitic capacitance becomes small.

[0178] In addition, by above-mentioned explanation, although existence of a pocket field is disregarded, retreat of the field Rpa shown in drawing 16 becomes remarkable in a pocket field existing. However, since the high-impurity-concentration profile fundamentally shown in drawing 16 is obtained even if it does not prepare a pocket field, there is an advantage which can simplify a process more.

[0179] In addition, although this

operation gestalt explained the case of Ti salicide process as a means of the reduction in resistance, the same effectiveness is expectable even if it applies the technique of others, such as a salicide process of others, such as Co and nickel, and a tungsten attachment technique by selection tungsten deposition.

[0180] In addition, boron and BF2 here As impregnation conditions, there is same effectiveness also on all conditions.

[0181] In addition, it is the same even when forming the diffusion layer which introduced all the impure sections, such as not only boron but Lynn, arsenic, in JUUMU, antimony, etc., as an impurity. Moreover, it is the same even when controlling diffusion of the impurity which does not form the diffusion layer of a fluorine etc.

[0182] In addition, about rapid heating heat treatment in an ammonia ambient atmosphere, the same effectiveness is expectable also in the ambient atmosphere of nitrogen, an argon, etc. However, it is thought desirable to introduce nitrogen as the 2nd different impurity from boron.

[0183] Furthermore, the same effectiveness is [be / it / not only a silicon substrate but under / polish recon / receiving] expectable.

[0184] In addition, although this operation gestalt explained the effectiveness at the time of introducing nitrogen into the extension field of a source drain field and a source drain field, there is effectiveness which controls diffusion of the impurity for carrier generation as well as this operation gestalt also about the case where nitrogen is introduced into a well or a channel field.

[0185] (9th operation gestalt) Drawing 18 (a) - (d) is the sectional view showing the production process of MOSFET concerning this operation gestalt.

[0186] First, at the process shown in drawing 18 (a), isolation 52 is formed in a part of silicon substrate 51, and gate oxide 53 and the gate electrode 54 are formed on the active region surrounded by isolation 52. The conditions at this time are the same as the gate oxide in each above-mentioned operation gestalt, and the conditions at the time of gate electrode formation, and good.

[0187] Next, at the process shown in drawing 18 (b), boron ion (B+) is poured in and the extension field 55 of a source drain is formed. The conditions at this time are the same as the conditions at the time of the extension formation in the operation gestalt of the above 8th, and conditions, and good.

[0188] Next, at the process shown in drawing 18 (c), nitrogen is introduced in a silicon substrate by heat-treatment in an ammonia gas ambient atmosphere. At this time, the processing time is made shorter than the processing time in the

8th operation gestalt, or processing temperature is made low so that high-concentration nitrogen may be introduced into a field shallower than the introductory field of the nitrogen in the operation gestalt of the above 8th. The nitrogen diffusion layer 55 is formed in the field near the front face of the extension field 55 of this processing. Simultaneously, the acid nitrated case 57 is formed in the both ends of gate oxide 53.

[0189] Next, at the process shown in drawing 18 (d), a sidewall 58 is formed on the both-sides side of the gate electrode 54, after that, in a silicon substrate, boron ion is poured in and the source drain field 59 is formed. The conditions at this time are the same as the time of the source drain formation in the operation gestalt of the above 8th, and good.

[0190] Then, the range of the extension field 56 and the source drain field 59 becomes settled by performing heat treatment for activation of an impurity.

[0191] In addition, it is desirable to perform after that the process which forms the silicide film on a source drain field and a gate electrode. However, it is not necessary to necessarily form the silicide film.

[0192] In this operation gestalt, since the comparatively high-concentration field in the extension field 55 is restricted near a front face, the pn junction section in a channel field can be made shallow, and channel resistance can be reduced. And since the acid nitrated case 57 is formed in the ends of gate oxide, it also has the advantage that improvement in the same effectiveness as the operation gestalt of the above 1st, i.e., dependability, can be aimed at. Moreover, when the silicide film is formed on a source drain field, it cannot be overemphasized like the operation gestalt of the above 8th that contact resistance can be made very small.

[0193] In addition, although this operation gestalt explained the case where the p mold MOSFET was formed, in case a silicon substrate is used as p mold substrate and a source drain field and an extension field are formed, the production process of the above-mentioned operation gestalt can be applied to the n mold MOSFET by pouring in arsenic ion. Also in such a case, since the pn junction section in a channel field can be made shallow, there is an advantage which can reduce channel resistance and can improve dependability.

[0194] Moreover, an impurity may be introduced in a substrate by nitrogen plasma treatment instead of performing heating heat treatment in an ammonia gas ambient atmosphere.

[0195] (10th operation gestalt) Drawing 19 (a) - (d) is the sectional view showing the production process of MOSFET concerning the 10th operation gestalt.

[0196] With this operation gestalt,

although it is the same as the operation gestalt and basic target of the above 9th, before forming the extension field 55, only the point which forms the nitrogen diffusion layer 56 differs from the operation gestalt of the above 9th. Also in this operation gestalt, the completely same effectiveness as the operation gestalt of the above 9th can be acquired, and the same deformation gestalt can be taken.

[0197] (11th operation gestalt) Drawing 20 (a) - (d) is the sectional view showing the production process of MOSFET concerning the 11th operation gestalt.

[0198] First, nitrogen is introduced into the field near the front face of the active region which forms isolation 52 in a part of silicon substrate 51, performs heat treatment in an ammonia gas ambient atmosphere in this condition, and is surrounded by isolation 52 at the process shown in drawing 20 (a). At this time, the processing time is made shorter than the processing time in the 8th operation gestalt, or processing temperature is made low so that high-concentration nitrogen may be introduced into a field shallower than the introductory field of the nitrogen in the operation gestalt of the above 8th. The nitrogen diffusion layer 55 is formed in the field near the front face of an active region of this processing. However, with this operation gestalt, since gate oxide is not formed yet at this process, the above 9th and the acid nitrated case 57 of the both ends of gate oxide [as / in the 10th operation gestalt] 53 are not formed.

[0199] Next, gate oxide 53 and the gate electrode 54 are formed on an active region at the process shown in drawing 20 (b). The conditions at this time are the same as the gate oxide in each above-mentioned operation gestalt, and the conditions at the time of gate electrode formation, and good.

[0200] Next, at the process shown in drawing 20 (b), boron ion (B+) is poured in and the extension field 55 of a source drain is formed. The conditions at this time are the same as the conditions at the time of the extension formation in the operation gestalt of the above 8th, and conditions, and good.

[0201] Next, at the process shown in drawing 20 (d), a sidewall 58 is formed on the both-sides side of the gate electrode 54, after that, in a silicon substrate, boron ion is poured in and the source drain field 59 is formed. The conditions at this time are the same as the time of the source drain formation in the operation gestalt of the above 8th, and good.

[0202] Then, the range of the extension field 56 and the source drain field 59 becomes settled by performing heat treatment for activation of an impurity.

[0203] In this operation gestalt, since the comparatively high-concentration field in a channel field and the extension field 55 is restricted near a front face, the pn

junction section in a channel field can be made shallow, and channel resistance can be reduced. Moreover, when the silicide film is formed on a source drain field, it cannot be overemphasized like the operation gestalt of the above 8th that contact resistance can be made very small.

[0204] In addition, although this operation gestalt explained the case where the p mold MOSFET was formed, in case a silicon substrate is used as p mold substrate and a source drain field and an extension field are formed, the production process of the above-mentioned operation gestalt can be applied to the n mold MOSFET by pouring in arsenic ion. Also in such a case, since the pn junction section in a channel field and an extension field can be made shallow, there is an advantage which can reduce channel resistance and can improve dependability.

[0205] Moreover, an impurity may be introduced in a substrate by nitrogen plasma treatment instead of performing heating heat treatment in an ammonia gas ambient atmosphere.

[0206] (12th operation gestalt) Drawing 21 (a) - (d) is the sectional view showing the production process of the vertical mold npn bipolar transistor concerning this operation gestalt.

[0207] At the process shown in drawing 21 (a), after introducing n mold impurity into the field near the front face of a silicon substrate 71 and forming the embedding collector layer 72 of n mold in it, n mold epitaxial layer 73 is formed on the whole surface of a substrate. Furthermore, after forming p mold detached core 74 in n mold epitaxial layer 73, deep n mold impurity is poured into the part in the field 75, i.e., a collector layer, surrounded by p mold detached core 74 by using photoresist film 81a as a mask, and the collector Wall layer 76 of n mold is formed in it.

[0208] Next, at the process shown in drawing 21 (b), after removing the above-mentioned photoresist film 81a, it heat-treats in an ammonia gas ambient atmosphere, and the nitrogen diffusion layer 77 is formed in the field containing the base layer specifically behind formed to a field deeper than the 8th operation gestalt. For the flow rate of ammonia gas, about 5 slm(s) and temperature are [about 950 degrees and the time amount of the heat treatment conditions at this time] about 30 sec extent. Next, low-concentration boron ion is poured into the part in a collector layer 75 by using photoresist film 81b as a mask, and the base layer 78 of p mold is formed. Impregnation energy is about 30 keV(s) and the dose of the conditions of the ion implantation at this time is abbreviation 2x1013cm-2.

[0209] Furthermore, by using photoresist film 81c as a mask, in the base layer 77 and the collector Wall layer 76,

high-concentration arsenic ion is poured in and the emitter layer 79 and the collector contact layer 80 of n mold are formed at the process shown in drawing 21 (c).

[0210] Then, heat treatment for activation is performed and the impurity introduced into each class is activated.

[0211] With this operation gestalt, since the nitrogen diffusion layer 77 is formed in the base layer 78, diffusion of the boron in the base layer 78 is controlled in the case of heat treatment for activation, comparatively, in high concentration, thickness is formed thinly, the base layer 78 is **, and base resistance becomes small. fT which gives the high frequency limitation of a common-emitter circuit It is D/W2, when width of face (this operation gestalt thickness) of a base region is set to W and a diffusion constant is set to D. Since it is known that it is proportional, it is the cut-off frequency fT of a bipolar transistor by the structure of this operation gestalt. The effectiveness that it can be made high can be demonstrated. Moreover, by the approach of this operation gestalt, since a nitrogen diffusion layer is formed also in an emitter layer, the concentration near the front face of an emitter layer can be raised, and there is an advantage that improvement in a current amplification factor can be aimed at by reduction of emitter resistance.

[0212] In addition, although this operation gestalt explained the example which formed the nitrogen diffusion layer in the base layer and the emitter layer, it cannot be overemphasized that a nitrogen diffusion layer may be formed only in the emitter layer or base layer of a bipolar transistor.

[0213] (Deformation gestalt about each operation gestalt) Before the processes shown in drawing 3 (a) in each above-mentioned operation gestalt, drawing 4 (a), drawing 5 (a), and drawing 6 (a), or those processes, it can heat in the gas containing nitrogen, such as nitrogen gas and ammonia gas, or plasma nitriding treatment can be performed, and nitrogen can be introduced in a silicon substrate. Also by this, the same effectiveness as the operation gestalt of the above 9th, 10, or 11 can be acquired. NH3 Heat treatment for 15 seconds is performed at 800 degrees C among a gas ambient atmosphere. By performing the same process as the process in each operation gestalt after that, the device which has the same configuration as each operation gestalt and a function can be formed. Also in other operation gestalten, it can replace with impregnation of nitrogen ion and the same effectiveness as each above-mentioned operation gestalt can be demonstrated by performing this processing.

[0214] In addition, the conditions of heat nitriding are N2. They are for 30 minutes or NH3 at the inside of a gas ambient

atmosphere, and 1000-1200 degrees C. Among a gas ambient atmosphere, if heat treatment for 10 - 30 seconds is performed at 600-800 degrees C, the acid nitrated case which has the same function as the 1st operation gestalt etc. can be formed into gate oxide.

[0215] The conditions of plasma nitriding are N2. For the flow rate of gas, 10 - 100ccm and gas pressure are [10 - 300mTorr and high-frequency power] about 50-300W. Then, the semiconductor device which has the same configuration as each operation gestalt and a function can be formed by performing the same process as the process in each operation gestalt.

[0216]

[Effect of the Invention] According to claims 1-8, as the semiconductor device which carried the MIS mold field-effect transistor, or its manufacture approach, since the acid nitrated case was prepared in the edge by the side of a drain at least, the dependability of gate oxide which does not almost have hot carrier degradation is high, and offer of a semiconductor device with the high engine performance without depletion-ization of the gate etc. can be aimed at.

[0217] According to claims 9-18, the nitrogen diffusion layer containing the nitrogen with which the defect resulting from the collision with a semi-conductor atom was introduced into the impurity diffused layer of a semi-conductor substrate in the condition below detection level is established. The impurity diffused layer which has this nitrogen diffusion layer The source drain field of an MIS mold field-effect transistor, an extension field, a channel field, etc., Or since it applied to a base region or an emitter region of a bipolar transistor etc., it has the impurity diffused layer which the high-concentration field concentrated, and offer of a semiconductor device with a sufficient property can be aimed at.

[0218] According to claims 19-33, as the manufacture approach of a semiconductor device of having carried the MIS mold field-effect transistor, since it was made the leaf of gate oxide which forms an acid nitrated case in the edge by the side of a drain at least, the dependability which does not almost have hot carrier degradation is high, and manufacture of a semiconductor device with the high engine performance without depletion-ization of the gate etc. can be aimed at.

[0219] Since the impurity diffused layer which introduces nitrogen so that the impurity diffused layer of a semi-conductor substrate may not be made to produce the defect more than the detection level resulting from the collision with a semi-conductor atom as the manufacture approach of a semiconductor device, and the high concentration field is concentrating was

formed according to claims 34-47, manufacture of a semiconductor device with a sufficient property can be aimed at.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the production process of the nMOS mold field-effect transistor concerning the 1st operation gestalt.

[Drawing 2] It is the sectional view showing the production process of the nMOS mold field-effect transistor concerning the 2nd operation gestalt.

[Drawing 3] It is the sectional view showing the production process of the CMOS device concerning the 3rd operation gestalt.

[Drawing 4] It is the sectional view showing the production process of the CMOS device concerning the 4th operation gestalt.

[Drawing 5] It is the sectional view showing the production process of the CMOS device concerning the 5th operation gestalt.

[Drawing 6] It is the sectional view showing the production process of the CMOS device concerning the 6th operation gestalt.

[Drawing 7] It is the sectional view showing the production process of the impurity diffused layer concerning the 7th operation gestalt.

[Drawing 8] The boron and BF2 who introduced nitrogen The boron and BF2 who have not introduced a diffusion layer and nitrogen It is drawing showing the concentration profile of a diffusion layer.

[Drawing 9] It is flow drawing showing the production process of the pMOS mold field-effect transistor concerning the 8th operation gestalt.

[Drawing 10] It is the sectional view showing the production process of the pMOS mold field-effect transistor concerning the 8th operation gestalt.

[Drawing 11] It is drawing showing the data about the gate length dependence property of the threshold for explaining the effectiveness about the 8th operation gestalt.

[Drawing 12] It is drawing showing the data about the saturation current property for explaining the effectiveness about the 8th operation gestalt.

[Drawing 13] It is drawing showing the data about the dependence property of the contact resistance to the area of the silicide-ized field interface for explaining the effectiveness about the 8th operation gestalt.

[Drawing 14] It is drawing showing the data about the gate width dependence property of the gate resistance of the n channel side transistor for explaining the effectiveness about the 8th operation gestalt.

[Drawing 15] It is drawing showing the data about the silicide width-of-face dependence property of the sheet resistance for explaining the effectiveness about the 8th operation gestalt.

[Drawing 16] It is a sectional view for explaining the difference with the source drain field of the pMOS mold field-effect transistor concerning the 8th operation gestalt, and the source drain field of the conventional pMOS mold field-effect transistor which pours in only boron and is obtained.

[Drawing 17] It is drawing for explaining the reason which the difference with the source drain field of the pMOS mold field-effect transistor concerning the 8th operation gestalt and the source drain field of the conventional pMOS mold field-effect transistor which pours in only boron and is obtained produces.

[Drawing 18] It is the sectional view showing the production process of the pMOS mold field-effect transistor concerning the 9th operation gestalt.

[Drawing 19] It is the sectional view showing the production process of the pMOS mold field-effect transistor concerning the 10th operation gestalt.

[Drawing 20] It is the sectional view showing the production process of the pMOS mold field-effect transistor concerning the 11th operation gestalt.

[Drawing 21] It is the sectional view showing the production process of the npn bipolar transistor concerning the 12th operation gestalt.

[Drawing 22] It is the sectional view showing the production process of the conventional nMOS mold field-effect transistor.

[Drawing 23] The boron in the source drain field of the conventional pMOS mold field-effect transistor, and BF2 It is drawing showing a concentration profile.

[Drawing 24] Conventional boron and BF2 It is drawing showing the Quasi-staticC-V property of a pMOS mold field-effect transistor of having the source drain field poured in and formed.

[Drawing 25] The conventional boron and conventional BF2 of flat band voltage of a pMOS mold field-effect transistor It is drawing showing an impregnation dose dependency.

[Description of Notations]

1 Silicon Substrate

2 Gate Oxide

3 Gate Electrode

4 Isolation

5 5a Acid nitrated case

6 6a Nitrogen diffusion layer

7 N Mold Low Concentration Source Drain Field

8 Sidewall

9 N Mold High Concentration Source Drain Field

10 Gate Top Oxide Film

12 P Mold Low Concentration Source Drain Field

13 P Mold High Concentration Source Drain Field

21 N Mold Silicon Substrate
22 P Mold Diffusion Layer
23 Boron and Nitrogen Mixture Layer (Nitrogen Diffusion Layer)
31 N Wells
32 Gate Oxide
33 Gate Electrode
34 Extension Field
35 Pocket Field
36 Insulator Sidewall
37 Source Drain Field
38 Boron and Nitrogen Mixture Layer (Nitrogen Diffusion Layer)
39 Silicide Film
40 Interlayer Insulation Film
41 Embedding Plug

[Translation done.]